



DATA SHEET

SV4E-DPTXCPTX

D-PHY / C-PHY Transmit Device Emulator

E SERIES



Table of Contents

Introduction	3
Overview	3
Key Features	3
Key Benefits	3
Physical Connections.....	4
QTH / QSH Connector	4
Additional Documentation	5
Ordering Information.....	5
Specifications	6

Introduction

OVERVIEW

The SV4E-DPTXCPTX is a highly integrated system-level tester that facilitates the rapid screening, calibration, and optimization of MIPI® enabled devices, including display panels, driver ICs, advanced image signal processors, and microcontrollers used in mobile and IoT applications. The SV4E-DPTXCPTX's unique dual-mode D-PHY/C-PHY analog front-end allows test engineers to perform multi-protocol validation. The SV4E-DPTXCPTX's excellent signal integrity allows design engineers to create realistic test setups where devices are run in conditions which are as close as possible to the end-user experience. The SV4E-DPTXCPTX operates with Introspect's easy-to-use, highly versatile Pinetree software environment which enables either interactive operation or full test automation.

KEY FEATURES

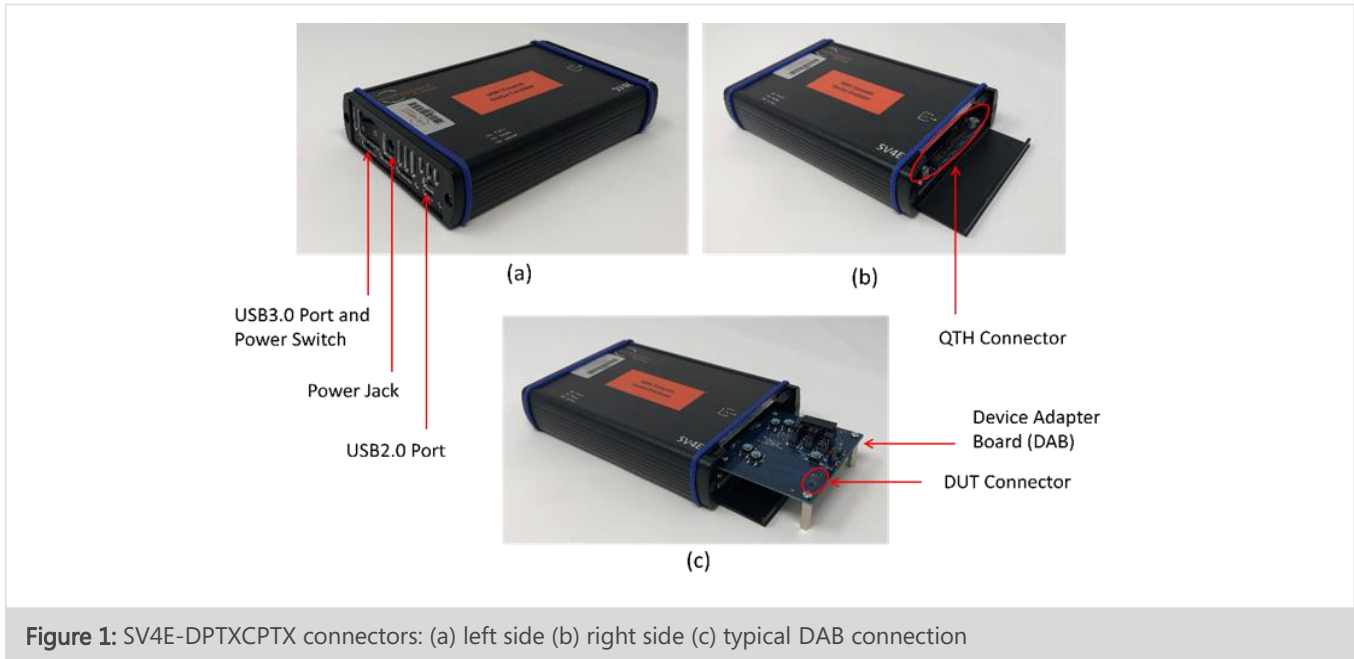
- **Dual Mode PHY:** Configurable as a D-PHY transmitter with up to four data lanes and clock or as a C-PHY transmitter with up to four trios
- **High Bandwidth:** Up to 2.5 Gbps D-PHY signaling and 2.5 Gbps C-PHY signaling
- **Native Protocol Implementations:** True CSI-2, DSI, and DSI-2 controller instantiations including escape-mode capability and bus turnaround (BTA)
- **GPIOs and I2C Master:** A total of 16 GPIOs including a built-in I2C controller allowing for full device emulation, all integrated within Pinetree
- **Programmable Power Supplies:** Six built-in power supplies for use with devices under test, with control and monitoring functions integrated within Pinetree

KEY BENEFITS

- **Future Proof:** Protect your investment by adopting a single tool for multiple product applications and MIPI standards.
- **Self-Contained:** An all-in-one system enables a true protocol handshake and helps create a system-oriented testing methodology.
- **Automated:** Scripting capability in Pinetree is ideal for debug tasks, firmware verification, and full-fledged production screening of devices and system modules.

PHYSICAL CONNECTIONS

Figure 1(a) and (b) show the ports and connectors on the SV4E-DPTXCPTX. The connection of a typical DAB is shown in Figure 1(c). The DAB provides the physical interface between the SV4E-DPTXCPTX to the DUT.



QTH / QSH CONNECTOR

The SV4E-DPTXCPTX has a 120 pin, high-speed connector for all inputs and outputs, with the following part number: Samtec QTH-060-01-L-D-A
<https://www.samtec.com/products/qth>

This part is designed to mate to a high-speed connector on the customer adapter board, using the following part number: Samtec QSH-060-01-L-D-A
<https://www.samtec.com/products/qsh>

For information on QTH signals and connections, please refer directly to the SV4E-DPTXCPTX Device Adapter Board Reference Design Guide, as listed in "Additional Documentation" on the following page.

ADDITIONAL DOCUMENTATION

SV4E-DPTXCPTX Device Adapter Board (DAB) Reference Design Guide

- **EN-G041E-E-23234** SV4E-DPTXCPTX Device Adapter Board (DAB) Reference Design Guide
 - Reference document for QTH / QSH pinout and general board design guidelines

SV4E-DPTXCPTX DAB Design Files.zip

- Includes reference schematic (.pdf), layout files (.brd) and Bill of Materials (.xlsx) for the example DAB. Please contact Introspect Technology for access to the reference design.

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV4E-DPTXCPTX

PART NUMBER	NAME	KEY DIFFERENTIATORS
5642	SV4E-CPTX MIPI C-PHY Transmitter	C-PHY, 4 trio transmit device emulator
5643	SV4E-DPTX MIPI D-PHY Transmitter	D-PHY, 4 lanes + clock transmit device emulator
5644	SV4E-DPTXCPTX Combo MIPI Transmitter	Combination D-PHY and C-PHY transmit device emulator (4 lanes + clock or 4 trios)

Specifications

TABLE 2: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	D-PHY C-PHY		
MIPI Protocol	CSI-2 v1.3, CSI-2 v2.0, DSI-2 v1.1 DSC v1.2 VDC-M v1.1		Flexible pattern architecture allows for the generation of encoded PHY data, unencoded PHY data, or entire CSI/DSI frames
LP/HS Handling	Automatic		
Ports			
Number of D-PHY Lanes	4 lanes and clock		
Number of C-PHY Trios	4 trios		
Number of GPIO pins *	16		
Pre-Defined GPIO pins *	4		SV4E Reset (input) I2C Bus (SCL, SDA, master only) Tearing Effect (input)
User-Defined GPIO *	12		Configurable, input or output, for use as triggers or flags Note: multiple SV4E instruments may be daisy-chained via GPIO to support multi-port operation
Programmable On-Board Power Supplies *	6		
Connections to PC for Pinetree Control	2		USB2 and USB3

* Please refer to the SV4E-DPTXCPTX Device Adapter Board (DAB) Reference Design Guide for additional details on GPIOs and on-board power supplies.

TABLE 3: MIPI TRANSMITTER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Output Coupling			
Output Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Output Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
Symbol Rates / Frame Rates			
Minimum Symbol Rate	156.25	Mbps	Per D-PHY lane Per C-PHY trio
	156.25	Msps	
Maximum Symbol Rate	2.5	Gbps	Per D-PHY lane Per C-PHY trio
	2.5	Gsps	
Minimum LP Toggle Rate	0	MHz	
Maximum LP Toggle Rate	20	MHz	
Packet Timing			
Minimum TLPX	50	ns	
Minimum T3-PREPARE	38	ns	
Minimum T3-PREBGIN	28	symbols	
Minimum T3-POST	7	symbols	

TABLE 4: HS VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
HS Voltage Performance			
Minimum Output Voltage Swing	130	mV	D-PHY, single ended C-PHY, single ended
Maximum Output Voltage Swing	287	mV	D-PHY, single ended C-PHY, single ended
Voltage Swing Resolution	5	mV	D-PHY, single ended C-PHY, single ended
Voltage Swing Accuracy	>10% or 15 mV	%, mV	
LP Voltage Performance			
LP Logic High Level	1200	mV	LP voltage control specifications apply to both D-PHY and C-PHY
LP Logic Low Level	0	mV	
Logic Level Accuracy	> 2% or 5 mV	%, mV	

TABLE 5: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Supported Pixel Formats			
Supported Pixel Formats (CSI)	RAW, RGB, YUV		RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, RGB444, RGB555, RGB565, RGB666, RGB888, YUV420, YUV422
Supported Pixel Formats (DSI)	RGB YCbCr		RGB101010, RGB121212, RGB332, RGB444, RGB565, RGB666, RGB888, YCbCr422_16bit, YCbCr422_20bit
Supported Features			
ALP support (CSI)	Yes		
EDP support (CSI)	Yes		
Display Command Set (DSI)	Yes		
Data Compression (DSI)	Yes		DSC v1.2, VDC-M v1.1
Data Scrambling (DSI)	Yes		Data payload and footer
Tearing Effect (DSI)	Yes		
Bus-Turn Around	Yes		CSI and DSI
Virtual Channel Support	Yes		CSI and DSI
Two-port operation	Yes		Multiple instruments can be daisy-chained via GPIO to support multi-port operation

TABLE 6: GPIO CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	1.8	V	All GPIOs operate at 1.8 V LVCMOS
V _{IL} minimum	-0.3	V	
V _{IL} maximum	0.7	V	
V _{IH} minimum	1.5	V	
V _{IH} maximum	2.2	V	
V _{OL} maximum	0.4	V	
V _{OH} minimum	1.7	V	

TABLE 7: PROGRAMMABLE POWER SUPPLY SPECIFICATION

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Performance			
Number of Programmable Power Supplies	6		Each supply programmed independently.
Minimum Voltage	1000	mV	
Maximum Voltage	5000	mV	
Voltage Programming Resolution	1	mV	
Maximum Output Current	3.0	A	
Current Measurement Capability	Yes		Independent measurement provided on each programmable supply.
Minimum Current Measurement	50	mA	
Current Measurement Resolution	4	mA	

TABLE 8: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	6.2, 158	in, mm	
Width	4.25, 108	in, mm	
Height	1.3, 34	in, mm	
Weight	1.5	lbs	
Physical Connections			
4 lanes and clock (D-PHY) 4 trios (C-PHY)	QTH		Available through QTH connector: Samtec QTH-060-01-L-D-A
GPIO pins	QTH		Available through QTH connector: Samtec QTH-060-01-L-D-A
Programmable Power Supplies	QTH		Available through QTH connector: Samtec QTH-060-01-L-D-A
PC connection	USB2 USB3		USB2.0 mini B USB3.0 micro B
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz
Power Consumption			
DC Input Voltage	12	Volt	
Current Draw	TBD	Amp	



REVISION NUMBER	HISTORY	DATE
1.0	Document Release	January 5, 2023
1.1	Updated software mentions to Pinetree	August 22, 2023

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