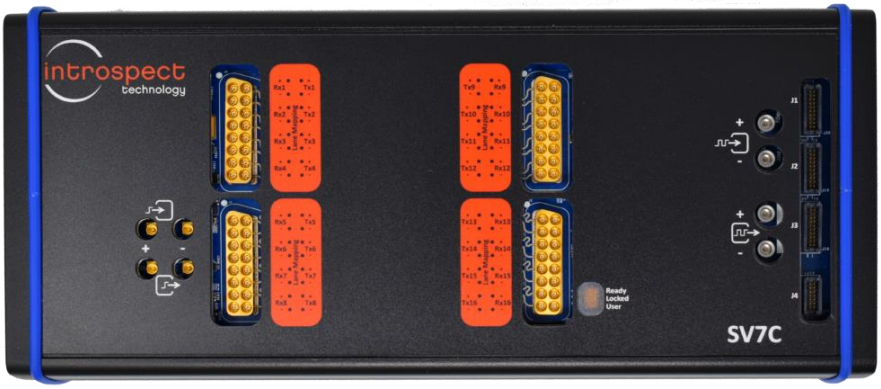
DATA SHEET

SV7C

Personalized SerDes Tester

C SERIES



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Introduction

OVERVIEW

The SV7C is a parallel high-speed tester that meets the emerging test and validation requirements of increasingly complex electronic component and board designs. Operating at up to 28 Gbps and featuring 16 independent pattern generators and 16 independent signal/data analyzers, the SV7C is an all-in-one, phase-aligned bit error rate tester (BERT) and protocol exerciser and analyzer, providing self-contained functional and physical layer test and measurement capabilities for interfaces such as DisplayPort, Thunderbolt, PCI Express, and others. The SV7C integrates multiple tools into one – a pattern generator with feed-forward equalization, an error detector with programmable equalization and clock recovery, a full-functional protocol exerciser, and a full-functional protocol analyzer. It provides unprecedented insights into crosstalk and channel-to-channel variations in highly parallel systems.

KEY BENEFITS

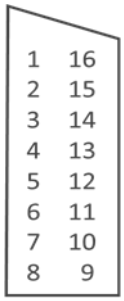
- High performance jitter tolerance testing in a handheld form factor
- Pattern generators offer per-lane voltage, timing, and noise injection controls
- Fully synthesized integrated jitter injection on all lanes
- Flexible pre-emphasis, equalization, and clock recovery per lane
- TX and RX phase alignment across all channels
- Protocol exerciser and analyzer features for DisplayPort v2.0 and PCI Express Gen4
- State of the art programming environment based on the highly intuitive Python language
- Single-ended or differential low-speed digital I/O for device under test control

APPLICATIONS

- DDR5, LPDDR5, and LPDDR5x protocol exercising and testing
- DisplayPort Version 2.0 receiver testing, protocol exercising, and protocol analysis
- USB 4.0 receiver and transmitter testing
- PCI Express 4.0 receiver and transmitter testing

MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: SIGNAL MAPPING OF THE MXP CONNECTORS FOR SV7C

	MXP1 PIN	MXP1 SIGNAL	MXP2 PIN	MXP2 SIGNAL	MXP3 PIN	MXP3 SIGNAL	MXP4 PIN	MXP 4 SIGNAL
MXP Top View 	1	RX1P	1	RX5P	1	RX9P	1	RX13P
	2	RX1N	2	RX5N	2	RX9N	2	RX13N
	3	RX2P	3	RX6P	3	RX10P	3	RX14P
	4	RX2N	4	RX6N	4	RX10N	4	RX14N
	5	RX3P	5	RX7P	5	RX11P	5	RX15P
	6	RX3N	6	RX7N	6	RX11N	6	RX15N
	7	RX4P	7	RX8P	7	RX12P	7	RX16P
	8	RX4N	8	RX8N	8	RX12N	8	RX16N
	9	TX4N	9	TX8N	9	TX12N	9	TX16N
	10	TX4P	10	TX8P	10	TX12P	10	TX16P
	11	TX3N	11	TX7N	11	TX11N	11	TX15N
	12	TX3P	12	TX7P	12	TX11P	12	TX15P
	13	TX2N	13	TX6N	13	TX10N	13	TX14N
	14	TX2P	14	TX6P	14	TX10P	14	TX14P
	15	TX1N	15	TX5N	15	TX9N	15	TX13N
	16	TX1P	16	TX5P	16	TX9P	16	TX13P

Features

TRANSMIT BUFFER

The transmit buffer in the SV7C is designed to enable full receiver test coverage while also allowing for maximum flexibility to interface to various device types. A simplified block diagram of the transmit buffer is shown in **Figure 1**. Each channel in the SV7C includes a programmable DC common-mode termination level, a programmable signal swing, and a programmable slew rate. Similarly, delay and noise generators enable fine static skew control, dynamic jitter control, and difference mode or common-mode AC noise control. Finally, each transmit buffer includes a 4-tap FIR filter for adjusting output signal waveform shape.

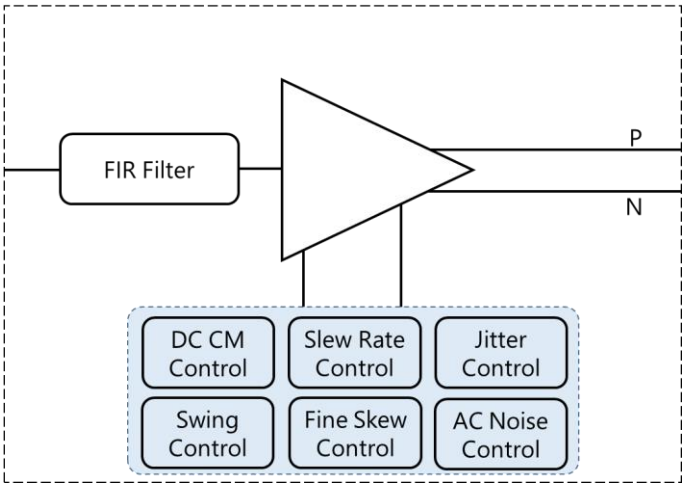


Figure 1: Transmit buffer controls in the SV7C

Each transmit buffer in the SV7C is programmed independently of other channels and independently of any pattern payload or functional protocol operation. This allows for automated receiver test sweeps under the most realistic conditions. For example, a receiver minimum sensitivity test can be performed on a subset of DisplayPort lanes while all neighboring signals are toggling at maximum voltage swing.

NOTE

The SV7C transmit buffer can operate in single-ended mode. Please refer to application-specific documentation for further information.

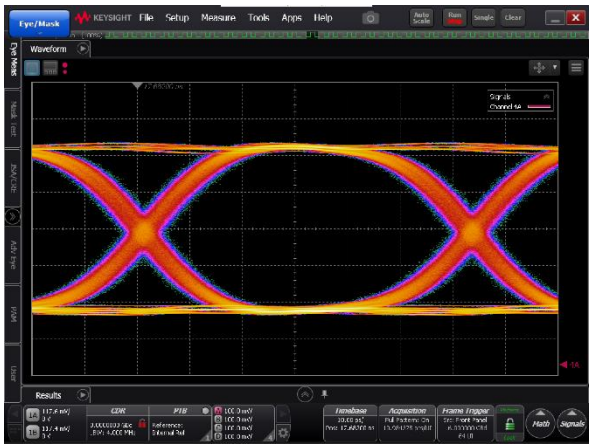


Figure 2: Illustration of the signal quality at the output of the SV7C transmit buffer

Figure 2 shows the quality of the output waveform of the SV7C pattern generators. Shown in the figure is a 16 Gbps PRBS pattern output. As can be seen, the eye diagram has a very flat voltage response, and this is a result of the rapid settling of the signal rise time.

RECEIVE BUFFER

Just like the transmit buffer, the SV7C receive buffer is designed to enable sophisticated signal measurement features while functionally interoperating with various device types and signaling interfaces. As shown in **Figure 3**, each receive buffer has a programmable continuous-time linear equalizer (CTLE) block, and this helps recover closed eyes at high data rates. More importantly, the receive buffer offers dynamic termination control, and it is able to operate in high-impedance mode while performing functional data captures. Finally, the SV7C receive buffer contains a window comparator with programmable threshold voltage and sampling phase controls.

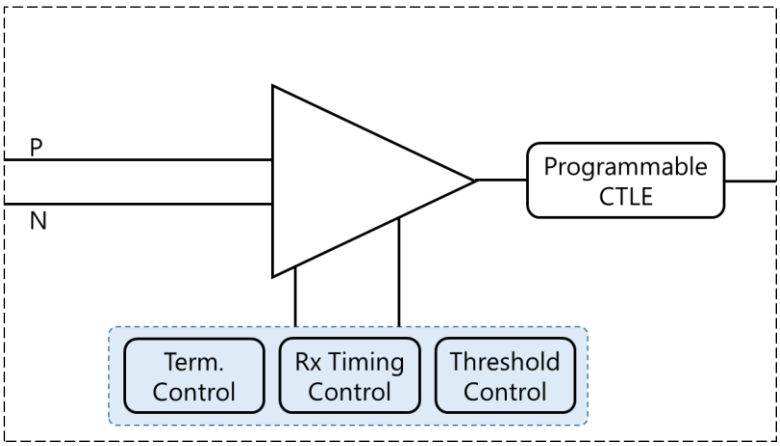


Figure 3: Receive buffer controls in the SV7C

Each receive buffer can be programmed independently of other channels and independently of any pattern payload that is being received. At the same time, the protocol capable machines inside the SV7C hardware and software are all able to automatically control the receive buffers, thus tremendously facilitating functional testing. That is, all receive buffer parameters are typically set automatically by the various pre-built functions in the SV7C and Pinetree.

SYSTEM CLOCKING

Figure 4 illustrates the global clocking network in the SV7C. A single reference clock source is used to drive the entire system, and this source can be internal or external (driven through the Clk In port). The master clock source is routed to three high-accuracy and low-jitter fractional-N synthesizers:

- Synth1 drives the main tester channels and provides the time base for all 16 transmit and receive channels
- Synth2 provides the ability to generate arbitrary external reference clocks that are synchronized to the Clk In port
- Synth3 provides the same capability as Synth2, thus resulting in two output reference clocks per SV7C

Each of the 16 tester channels contains precision timing synthesis blocks that are used for generating frequency drifts, static skews, dynamic skews (and jitter), and bit slips.

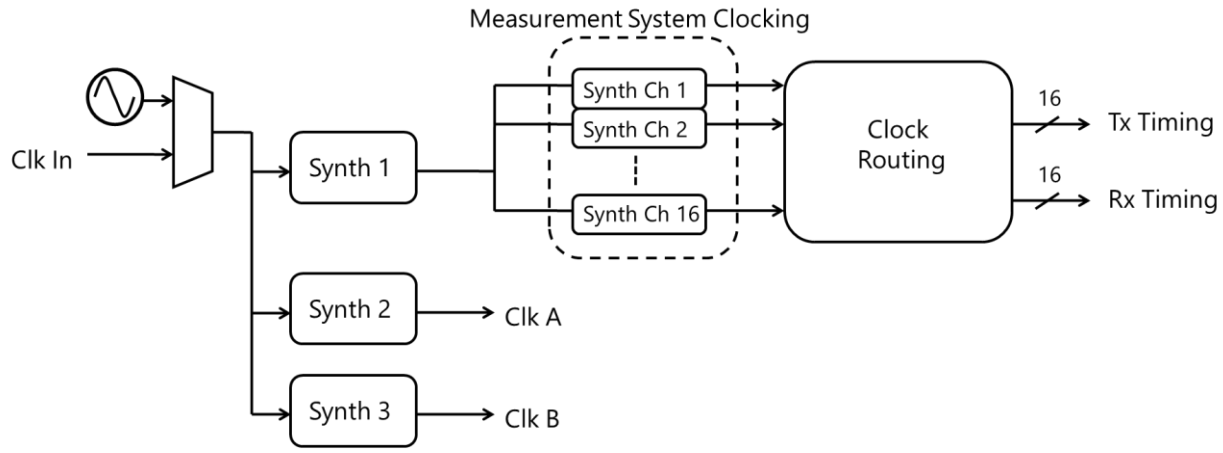


Figure 4: Global clock network in the SV7C

PATTERN AND PROTOCOL HANDLING

The SV7C contains several pattern provider tools for generating and/or receiving test patterns. At the basic fixed-pattern level, the SV7C can generate any PRBS polynomial as well as any user-defined pattern. In addition, the SV7C contains nested pattern sequencers in which 16 separate pattern blocks can be programmed with arbitrary repetition counts and then these repeated blocks can be inserted into an outer repetition loop.

Perhaps most importantly, the SV7C contains protocol aware features that allow for the creation of functional command sequences. These features are encapsulated in Pattern Timeline tools, an example of which is shown in **Figure 5**. This tool contains repeats, pauses, branched commands, and triggers based on received protocol traffic or received programming commands. The net result is that the SV7C can perform complete functional testing, thus resulting in a highly effective ATE-on-Bench solution for wide-bus applications.

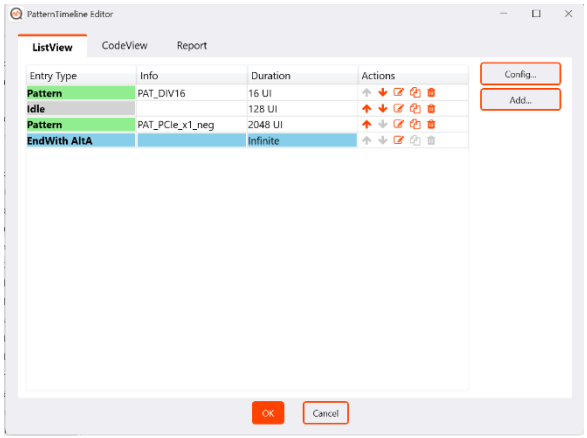


Figure 5: Pattern timeline editor illustrating the ability to create complex timing and command sequences

Finally, where appropriate, complete protocol solutions are available. For example, for DisplayPort receiver testing, a complete DisplayPort Generator component is available in the software, and it allows for the generation of arbitrary video streams and for the complete protocol exercising of DisplayPort sink devices. **Figure 6** shows the built-in DisplayPort generator component class in Introspect's Pinetree software. With this component, video and audio files can be imported into the software and then streamed through the SV7C with a full suite of protocol and physical layer capability.

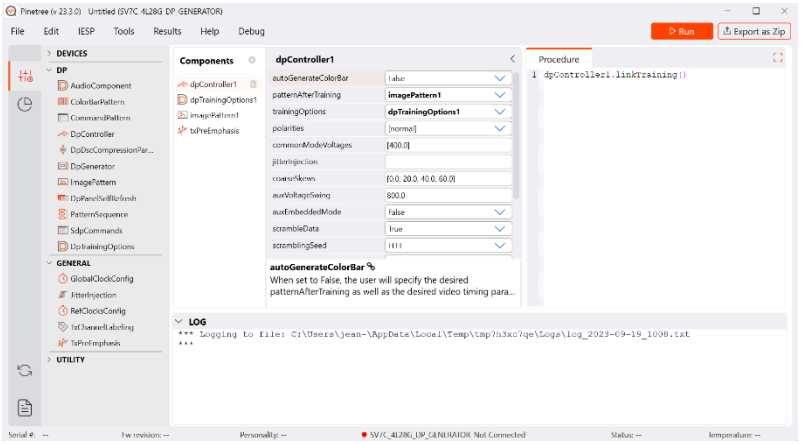


Figure 6: Built-in DisplayPort generator component

STANDARD ERROR DETECTOR ANALYSIS

The SV7C instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (using the per-channel CDR) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Shmoos of various kinds

Figure 7 illustrates a few of the analysis and reporting features of the SV7C. Starting from the top left and moving in a clockwise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, eye diagram plotting and raw data viewing. As always, these analysis options are executed in parallel on all activated lanes.

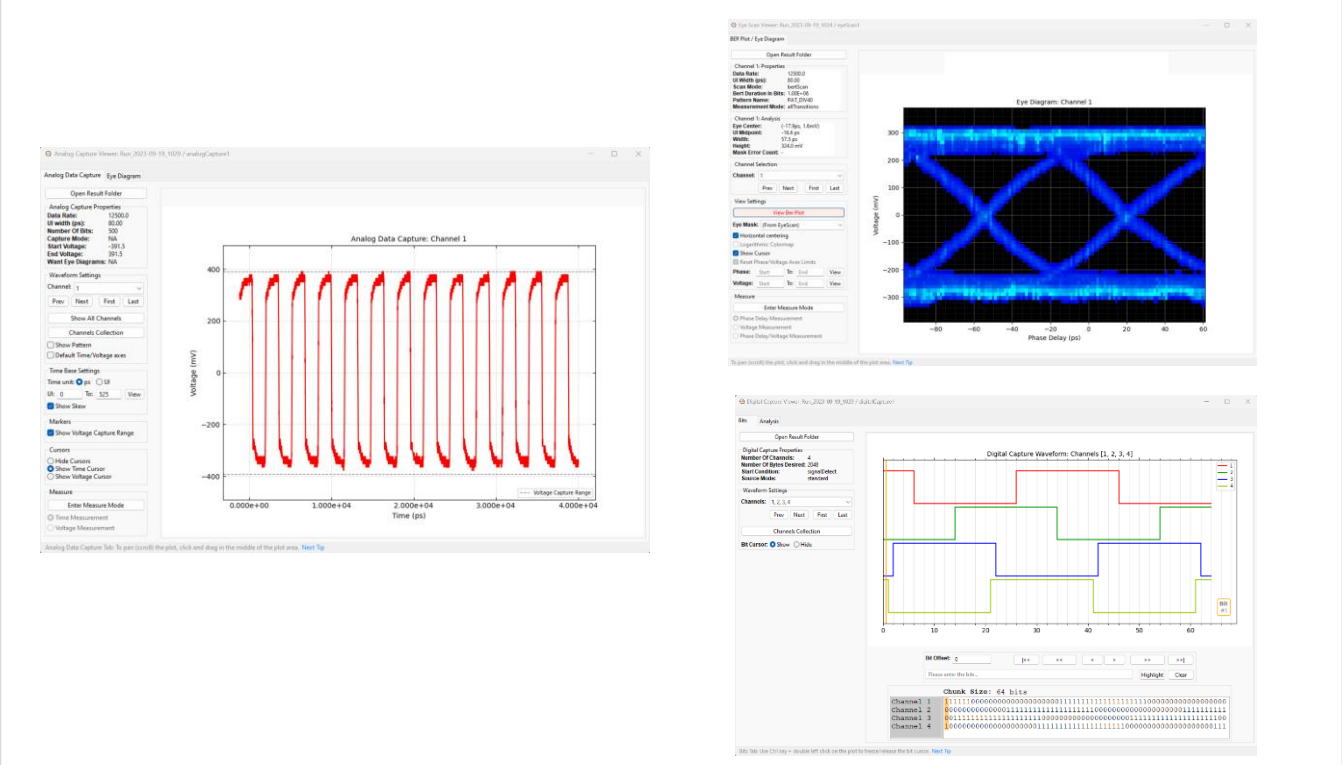


Figure 7: Collection of standard error detector tools in the SV7C

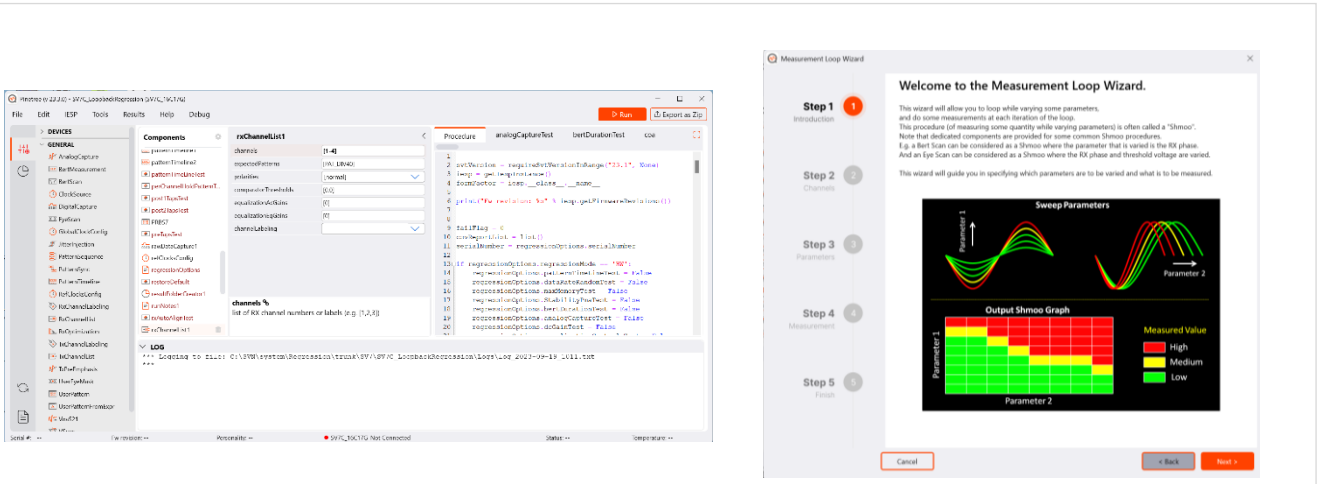
AUXILIARY DEVICE CONTROLS

The SV7C contains general purpose I/O pins for controlling devices under test or driving sideband bus signals. Of these pins, the following classes of functions are available:

- Trigger and flag pins for starting patterns, capturing patterns, or reporting test results
- I2C/I3C master pins (SDA/SCL) for controlling devices such as DDR5 power management integrated circuits (PMIC) or sensors
- Daisy-chain trigger in and trigger out pins for cascading and aligning multiple SV7C units together. These daisy chain signals work in conjunction with the Clk In, Clk A, and Clk B signals to align any number of SV7C units together

AUTOMATION

The SV7C is operated using Introspect's award-winning software, Pinetree. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in **Figure 8**(a). Component-based design is Pinetree's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV7C features wizard-based code generation for highly automated tasks such as measurement loops (illustrated in **Figure 8**(b)).



(a) (b)

Figure 8: Screen captures of the Pinetree software

Specifications

TABLE 2: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of Transmitters	16		Capable of single-ended operation
Number of Receivers	16		Capable of single-ended operation
Number of Dedicated Clock Outputs	2		Individually synthesized frequency and output format
Number of Dedicated Clock Inputs	1		Used as external reference clock input
Number of Trigger Inputs	2		
Number of Flag Outputs	2		
Number of I2C/I3C Masters	1		
Power			
DC Input Voltage	12	Volt	
Current Draw	12	Amp	1 Gb6ps / 16 channel TX and RX operation
	TBD	Amp	28 Gbps / 16 channel TX and RX operation
Data Rates and Frequencies			
Minimum Programmable Data Rate	400	Mbps	
Maximum Programmable Data Rate	28	Gbps	
Maximum Data Rate Purchase Options	17 28	Gbps Gbps	
Data Rate Field Upgrade	Yes		License to change speed grade is available for purchase at any time
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization

Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	500	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 3: TRANSMIT BUFFER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Output Coupling			
Output Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Output Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
Output Voltage Performance			
Minimum Single-Ended Voltage Swing	0	V	Can achieve true idle signaling
Maximum Single-Ended Voltage Swing	400	mV	
Voltage Swing Resolution	10	mV	
Voltage Swing Accuracy	>10% or 10 mV	%, mV	
Minimum Common Mode Voltage	-20	mV	
Maximum Common Mode Voltage	900	mV	

Common Mode Voltage Resolution	1	mV	
Common Mode Voltage Accuracy	>20% or 20 mV	%, mV	
Swing and Common Mode Setting	Per Lane		
Rise Time	17	ps	
Fall Time	17	ps	
Slew Rate Range	TBD	V/ns	This is defined as the difference between the fastest slew rate and the slowest slew rate
De-Emphasis Performance			
Pre-Tap 1 Range	+/- 150	mV	FIR taps defined as additive increments
Pre-Tap 1 Resolution	10	mV	
Post-Tap 1 Range	+/- 300	mV	
Post-Tap 1 Resolution	10	mV	
Post-Tap 2 Range	+/- 150	mV	
Post-Tap 2 Resolution	10	mV	
De-Emphasis Setting	Per Lane		
Jitter and Noise Performance			
RJ (RMS)	700	fs	Based on a sampling oscilloscope measurement with first order clock recovery
Minimum Frequency of SJ	0.1	kHz	
Maximum Frequency of SJ	50	MHz	The jitter injection at 50 MHz is limited to only 40 ps.
Frequency Resolution of SJ	0.1	kHz	
Maximum Peak to Peak SJ	16000	ps	Test limit – functional limit can be much higher.
Magnitude Resolution of SJ Programming	500	fs	
Accuracy of Injected SJ	>10% or 10 ps	%, ps	
Number of SJ Sources per Channel	2		

Maximum Amplitude of Common Mode Noise	40	mV	
Maximum Amplitude of Difference Mode Noise	80	mV	
Amplitude Resolution of Injected Noise	1	mV	
Maximum Frequency of Injected Noise	1	GHz	
Channel Skew Performance			
Minimum Coarse Skew	-20	UI	
Maximum Coarse Skew	+20	UI	
Coarse Skew Resolution	0.5	UI	Data rates < 6.25 Gbps
Coarse Skew Resolution	1	UI	Data rates >= 6.25 Gbps
Minimum Fine Skew	-500	ps	Testing limit – hardware is capable of larger skews
Maximum Fine Skew	+500	ps	Testing limit – hardware is capable of larger skews
Fine Skew Resolution	1	ps	
Channel to Channel Auto Alignment Accuracy	20	ps	Across 16 channels

TABLE 4: RECEIVE BUFFER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Input Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
High-Impedance Programming	Per Lane		Dynamically programmable within Pattern Timeline
Comparator Performance			

Minimum Threshold Voltage	-400	mV	
Maximum Threshold Voltage	+400	mV	
Threshold Voltage Resolution	20	mV	
Threshold Voltage Accuracy	>15% or 15 mV	%, mV	
Minimum Detectable Differential Voltage	90	mV	
Maximum Allowable Differential Voltage	1200	mV	
Resolution Enhancement			
DC Gain Settings	0, 3, 6, 8, 10	dB	
CTLE High Frequency Settings	0 … 15	dB	
DC Gain Settings	Per Lane		
CTLE Settings	Per Lane		
Receiver Jitter Performance			
RMS Jitter Noise Floor (<6.25 Gbps)	2	ps	RMS
RMS Jitter Noise Floor (>6.25 Gbps)	1	ps	RMS
Timing Generator Performance			
Timing Resolution	7.8125	mUI	Measured at 12.5 Gbps
	3.90625	mUI	Measured at 6.25 Gbps
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		

TABLE 5: CLOCKING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	kbps	
Clock Recovery			
Tracking Bandwidth	20	MHz	
Clock Recovery Setting	Per Lane		Can be disabled for source synchronous applications
SSC Tracking Bandwidth	66	kHz	
SSC Tracking Spread	0.5	%	

TABLE 6: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
PRBS Patterns			
Polynomials	5,7,9,11,13,15,21,31		
PRBS Generator Setting	Per Lane		
Pattern Sequencer			
Entry and Exit Slots	Yes		
Number of Inner Slots	16		
Repeat Count Per Slot	65536		
Repeat Count for Outer Loop	65536		Outer loop can encompass any number of slots, up to all 16 slots
Pattern Timeline			
Hold States	Alt A		
	Alt B		

	All Ones		
	All Zeros		
	Idle		
	Wait for Trigger		
	Wait for Received Word		
	Wait for Software Command		
Hold State Setting	Per Lane		
Memory			
Total Space for Pattern Storage	8	GBytes	Memory sustains full bandwidth streaming on all 16 transmitters and 16 receivers simultaneously
Protocol Pattern Handling			
Clock-Forwarded Interfaces	DDR5, LPDDR5, LPDDR5x		For subsequent evolved protocols, such as DDR6/LPDDR6, pure software upgrades are supported but the customer shall pay for the software upgrades in the future.
Embedded Clock Interfaces	USB, DisplayPort, PCI Express		

REVISION NUMBER	HISTORY	DATE
1.0	Document release	October 27, 2021
1.1	Updated software screenshots and featured image	September 21, 2023

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