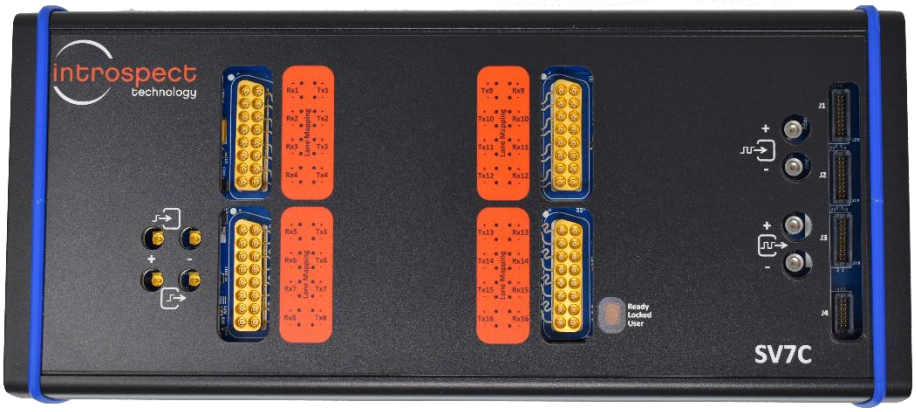
DATASHEET

SV7C-eDP Generator

Embedded DisplayPort Generator

C SERIES



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Introduction

OVERVIEW

The **SV7C-eDP Embedded DisplayPort Generator** is an ultra-portable, high-performance instrument capable of generating traffic for Embedded DisplayPort and DisplayPort applications. The SV7C-eDP Generator provides analog parameter controls that enable DisplayPort receiver stress-testing and allow for deep insights into voltage and timing sensitivities of DisplayPort sink devices. The instrument operates with the award-winning Introspect ESP Software environment which includes full pattern synthesis tools for generating test patterns and video frames for system-level test. Figure 1 below illustrates a typical application of the SV7C-eDP Generator in an Embedded DisplayPort system.

KEY FEATURES

- **Protocol**: supports Embedded DisplayPort (**eDP**) up to v1.5 and DisplayPort (**DP**) up to v2.1
- **Supported Data Rates:** up to 26 Gbps with a fully continuous range of data rates
- **Lane Count:** configurable from 1 to 4 lanes (ML1 to ML4) plus auxiliary channel (AUX)
- **Analog Controls:** voltage amplitude and common mode voltage, each per lane
- **Signal Impairments:** jitter injection, sinusoidal voltage noise injection, per-wire timing skew
- **Pattern Generation:** full video frame generation with 8 GBytes of total pattern memory

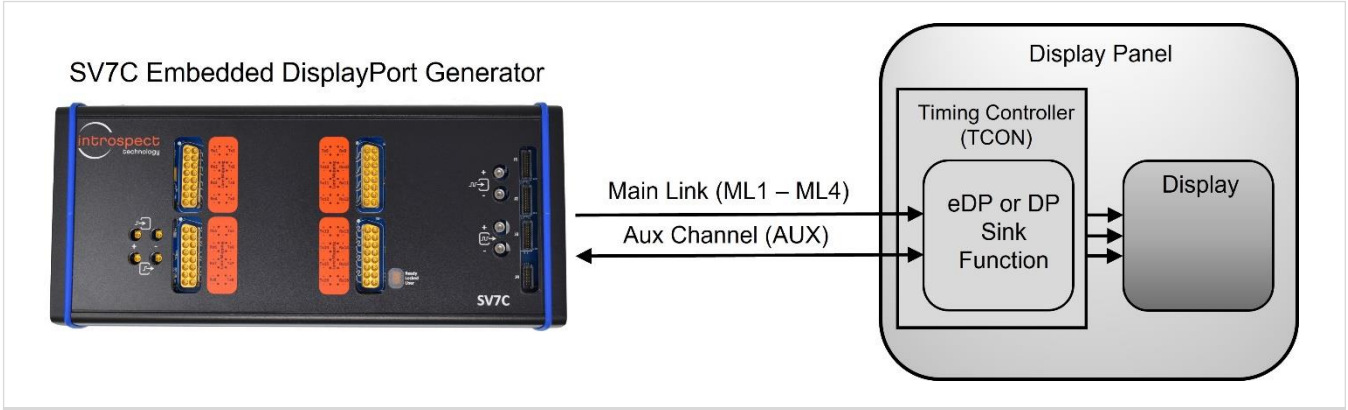


Figure 1: Typical application of the SV7C-eDP Generator connected to an Embedded DisplayPort system.

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV7C-EDP ANALYZER WITH RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5941	SV7C-eDP Generator (includes Introspect ESP Software license)	High performance eDP protocol generator and sink tester
5942	SV7C-eDP Analyzer (includes Introspect ESP Software license)	High performance eDP protocol analyzer and source tester

Physical Connections

SV7C-EDP GENERATOR

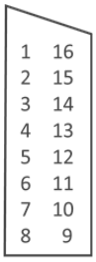
The physical connections of the SV7C-eDP Analyzer are shown in Figure 2.

Figure 2: SV7C-eDP physical connections.

MXP MAIN LINK CONNECTOR

The Main Link signals are located on the upper left MXP connector as shown in Figure 2 on the previous page and the full pinout description as given in Table 2 below.

TABLE 2: UPPER MXP CONNECTOR PINOUT

CONNECTOR	PIN	SV7C LABEL	EDP LANE
	16 15	Tx1+ Tx1-	ML Lane 1P ML Lane 1N
	14 13	Tx2+ Tx2-	ML Lane 2P ML Lane 2N
	12 11	Tx3+ Tx3-	ML Lane 3P ML Lane 3N
	10 9	Tx4+ Tx4-	ML Lane 4P ML Lane 4N

MXP AUXILIARY CHANNEL CONNECTOR

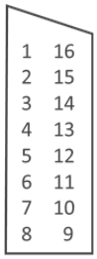
The Auxiliary Channel signals are located on the lower left MXP connector as shown in Figure 2 on the previous page. The full pinout description of the Auxiliary Channel is given in Table 3 on the following page. Note that the Auxiliary Channel in DisplayPort is bi-directional, and as such there are separate MXP connections for the TX signal (the generator / source controls the Auxiliary Channel) and the RX signal (the generator / source receives from the Auxiliary Channel).

Combiner circuits which are external to the SV7C-eDP Generator are required between the Auxiliary Channel TX pins and the Auxiliary Channel RX pins. Figure 3(a) shows the required connections between the eDP or DP source, the external combiner, and the SV7C-eDP.

The SV5C-eDP Generator is provided with external combiner circuits such as shown in Figure 3(b). The intended pinout for each port is as shown in the figure, though note that this resistive combiner is entirely symmetric, so the port mapping is not critical.

Alternatively, off-the-shelf components such as MiniCircuits ZFRSC-42-S+, as shown in Figure 3(c), can be used as the external combiner circuit.

TABLE 3: AUXILIARY CHANNEL MXP CONNECTOR PINOUT

CONNECTOR	PIN	SV7C LABEL	LANE
	16	Tx5+	Auxiliary Channel P, TX
	15	Tx5-	Auxiliary Channel N, TX
	1	Rx5+	Auxiliary Channel P, RX
	2	Rx5-	Auxiliary Channel N, RX

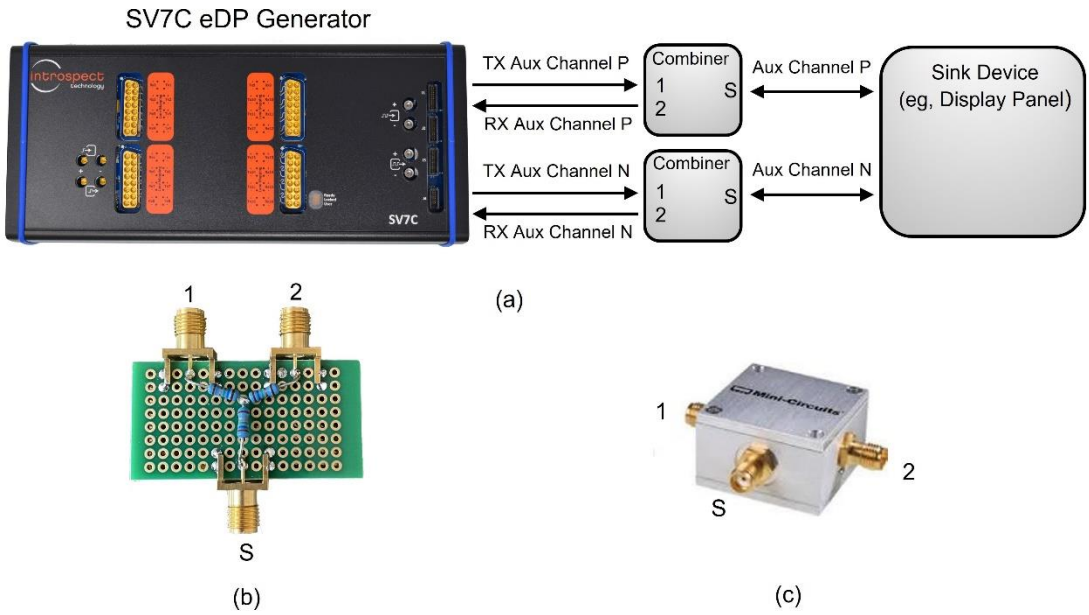


Figure 3: (a) Connection of bi-directional Auxiliary Channels between the SV7C eDP Generator and a Sink device, (b) an example of the provided external combiner circuit (c) the off-the-shelf MiniCircuits ZFRSC-42-S+ combiner circuit

Specifications

TABLE 4: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	eDP DP		Support for eDP to version 1.5 Support for DP to version 2.1
Ports			
Number of Generator Lanes	5		ML1 to ML4 Aux Channel (bidirectional)
Number of GPIO pins	30		Programmable as external trigger input or flag output pins
Number of dedicated reference clock inputs	1		
Number of dedicated reference clock outputs	1		
PC connections for Introspect ESP Software Control	2		USB2 and USB3 Type-C
Data Rates and Reference Clocks			
Minimum Data Rate	1.0	Gbps	Per Lane
Maximum Data Rate	26	Gbps	Per Lane
Minimum External Input Ref Clock	10	MHz	
Maximum External Input Ref Clock	250	MHz	
Minimum External Output Ref Clock	10	MHz	
Maximum External Output Ref Clock	500	MHz	
Power Consumption			
DC Input Voltage	12	V	
Power Dissipation	TBD	W	

TABLE 5: EDP TRANSMITTER LANE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
HS Voltage Performance			
Minimum Output Voltage Swing	20	mV	Differential
Maximum Output Voltage Swing	850	mV	Differential
Voltage Swing Resolution	10	mV	Differential
Voltage Swing Accuracy	10% or 10 mV		The larger value of 10% or 10 mV
Minimum Common Mode Voltage	100	mV	
Maximum Common Mode Voltage	750	mV	
Common Mode Voltage Resolution	1	mV	
Common Mode Voltage Accuracy	20% or 20 mV		The larger value of 20% or 20 mV
Swing and Common Mode Setting	Per Lane		
HS Timing Performance			
Rise and Fall Time	20	ps	Typical, fastest slew rate setting 20% to 80%
Slew Rate Range	TBD	V/ns	Difference between the fastest slew rate and the slowest slew rate
De-Emphasis Performance			
Pre-Tap 1 Range	+/- 150	mV	FIR taps defined as additive increments
Pre-Tap 1 Resolution	10	mV	
Post-Tap 1 Range	+/- 300	mV	
Post-Tap 1 Resolution	10	mV	
De-Emphasis Setting	Per Lane		
Transmitter Lane Output Coupling			
Output Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	

TABLE 6: EDP TRANSMITTER SIGNAL IMPAIRMENT CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Noise Floor			
Random Jitter (RMS)	< 1.2	ps rms	
Deterministic Jitter Injection			
Minimum Sinusoidal Frequency	0.1	kHz	Per lane
Maximum Sinusoidal Frequency	50	MHz	Per lane
Frequency Resolution	0.1	kHz	
Maximum Sinusoidal Amplitude	16000	ps	Peak-Peak, tested to 1000 ps
Sinusoidal Amplitude Resolution	500	fs	
Sinusoidal Amplitude Accuracy	10% or 10 ps		The larger value of 10% or 10 ps
Voltage Noise Injection			
Maximum Amplitude of Common Mode Noise	40	mV	
Maximum Amplitude of Difference Mode Noise	80	mV	
Amplitude Resolution of Injected Noise	1	mV	
Maximum Frequency of Injected Noise	1	GHz	
Channel Skew Performance			
Coarse Skew Range: Programmable Skew	 +/- 20	 UI	Lane to lane Hardware is capable of larger skews
Coarse Skew Resolution: 1.62 Gbps 2.7 Gbps 5.4 Gbps, 8.1 Gbps 10.0 Gbps, 13.5 Gbps, 17.4 Gbps	 0.125 0.25 0.5 1	 UI UI UI	Lane to lane
Fine Skew Range: Programmable Skew	 +/- 500	 ps	Wire to wire and lane to lane Hardware is capable of larger skews

TABLE 7: PATTERN MEMORY AND FRAME FEATURES

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
User-Programmable Pattern Memory			
Minimum Pattern Segment Size	8	Bits	
Maximum Pattern Segment Size	8	GBytes	
Total Transmitter Memory Space	8	GBytes	
Frame Features and Formats			
Frame Modes	Standard Enhanced		
Supported Pixel Formats	RAW RGB YCbCr		RAW6, RAW8, RAW9, RAW10, RAW11, RAW12, RAW14, RAW16 RGB666, RGB888, RGB999, RGB101010, RGB111111, RGB121212, RGB161616 YCbCr422, YCbCr444 and Y-Only at: 6 bit, 8 bit, 9 bit, 10 bit, 11 bit, 12 bit and 16bit
Supported YCbCr Standard	YCbCr601 YCbCr709		
Data Scrambling Support	Yes		
Scrambling Seed	FFFE FFFF		Up to eDP/DP v1.5
Forward Error Correction (FEC)	Yes		
Advanced Link Power Management (ALPM) Support	Yes		
Panel Self Refresh With Selective Update (PSR2) Support	Yes		

TABLE 8: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	10.75, 273	in, mm	
Width	4.92, 125	in, mm	
Height	2.20, 56	in, mm	
Weight	5	lbs	
Physical Connections			
ML1 to ML4, Aux Channel	MXP		Huber & Suhner, 16 pin
GPIO			Available through 14 pin and 20 pin headers, with connector part numbers: Samtec TFM-107-01-X-D Samtec TFM-110-01-X-D
Ref Clock In	SMP		SMP Differential Pair
Ref Clock Out	SMP		SMP Differential Pair
High Speed Trigger Pins	MMPX		MMPX Differential Pair
High Speed Clock Output Pins	MMPX		MMPX Differential Pair
PC connection	USB2 USB3		USB2.0 mini B USB3.0 Type-C
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz

Revision Number	History	Date
1.0	Document Release	November 7, 2022

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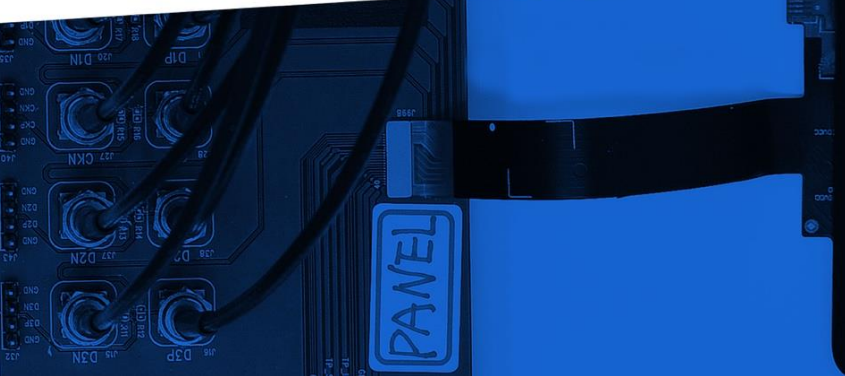

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