SV2C Personalized SerDes Tester

Data Sheet

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Introduction

Overview

The **SV2C Personalized SerDes Tester** is an ultra-portable, high-performance instrument that creates a new category of tool for testing high-speed digital products. The SV2C integrates multiple technologies to enable self-contained test and measurement of SerDes up to 32 Gbps. Coupled with a seamless, easy-to-use development environment, the SV2C enables product, validation and production test engineers to develop fast, efficient SerDes verification algorithms. The SV2C fits in one hand and contains eight independent stimulus generation ports, eight independent error detectors and various clocking, synchronization and lane-expansion capabilities. It has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection, de-emphasis generation, and equalization.

With a small form factor, an extensive feature set, and an exceptionally powerful software development environment, the SV2C is not only suitable for receiver signal-integrity verification engineers that perform traditional characterization tasks, but it is also ideal for FPGA developers and software developers who need rapid turnaround signal verification tools or hardware-software interoperability confirmation tools.

Key Benefits

- True parallel bit-error-rate measurement across 8 lanes
- Continuous data rate selection from 1 Gbps - 32 Gbps
- Fully-synthesized integrated jitter injection on all lanes
- Programmable output voltage for receiver stress test applications
- Two-tap pre-emphasis control
- Capability to measure eye diagrams, bathtub plots and BER
- Flexible loopback support per lane
- Hardware clock recovery per lane
- State of the art programming environment based on the highly intuitive Python language
- Reconfigurable, protocol customization (on request)

Applications

- Parallel PHY validation of serial bus standards
- Parallel PHY validation and eye margining
- Interface tests of electrical/optical media
- Passive device testing
- At-speed production tests

Features

Flexible Operating Modes

The SV2C is a compact, versatile test instrument replacing multiple pattern generators and receivers of a traditional testbench. Eight differential high-speed pattern generators are available each with independent pattern, pre-emphasis and amplitude controls. Eight differential high-speed receivers each with their own CDR capture and analyze incoming data. Transmit and receive channels can operate either concurrently or independently as illustrated in Figure 1. For active devices with, and without, internal logic and passive device testing the SV2C is a complete, self-contained test solution. For multi-lane SerDes at 32 Gbps, the SV2C enables unprecedented at-speed testing for measurement of true device performance.

The SV2C is controlled via the award-winning Introspect ESP GUI, built with Python to integrate seamlessly into modern validation laboratories. Using the open Introspect ESP Python libraries and an available .NET DLL library the PC and the SV2C seamlessly integrate with DUT command interfaces for fast, automated testing as illustrated in Figure 1(b)-(c).

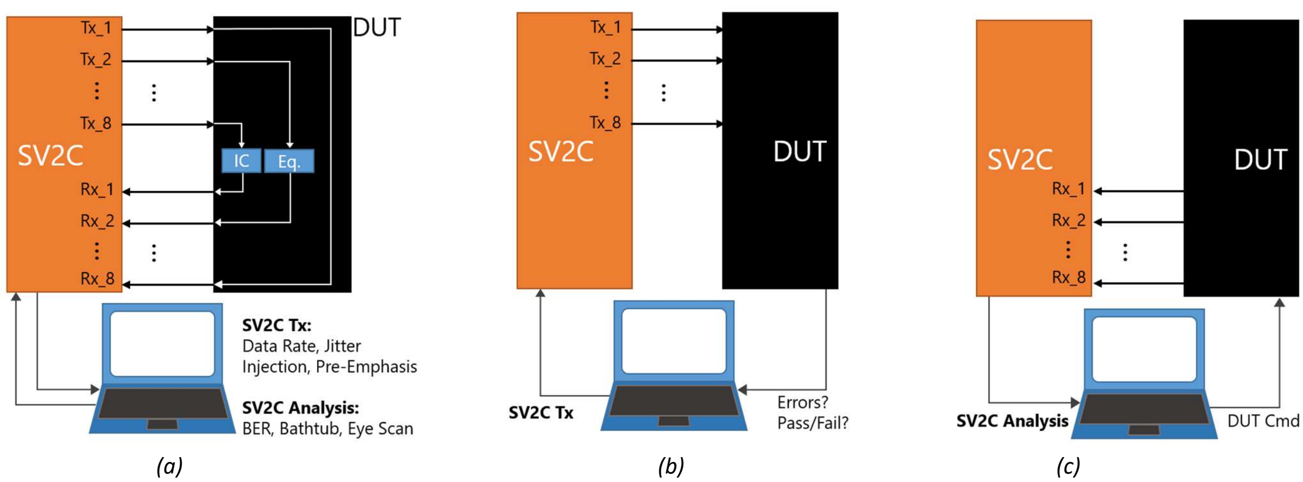


Figure 1. Three typical use-cases: (a) SV2C Tx and Rx exercising DUT loopback circuitry: IC, equalizer (active pass-through device) and interconnect trace (passive device), (b) SV2C driving DUT and PC receives pass/fail flags from DUT internal evaluation function, (c) SV2C capturing and analyzing data transmission from DUT

Multiple-Source Jitter Injection

The SV2C is capable of injecting calibrated, multi-UI jitter amplitudes over a range of SJ frequencies that cover various receiver CDR bandwidths. An example is illustrated in Figure 2 in which 5 UI jitter is injected at 25 Gbps. Given that most oscilloscopes are not able to recognize large jitter amounts, the measurement in the figure is made by programming a DIV10 pattern on the transmitter of the SV2C (the SV2C pattern generators are capable of creating arbitrary custom patterns).

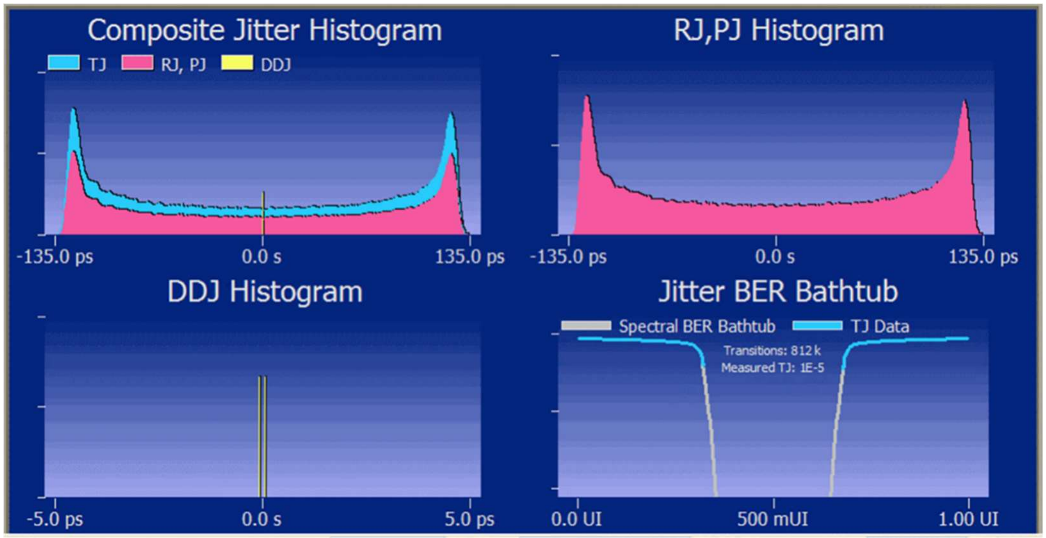


Figure 2. Multi-UI jitter injection at 25Gbps (viewed on a DIV10 pattern)

Pre-Emphasis Generation

Per-lane pre-emphasis control is integrated to the SV2C. The user can individually set the transmitter pre-emphasis using a built-in Tap structure. Pre-emphasis allows the user to optimize signal characteristics at the DUT input pins for creating best- and worst-case scenarios and emulating DUT transmitters.

Each transmitter in the SV2C implements a discrete-time linear equalizer as part of the driver circuit. An illustration of such equalizer is shown in Figure 3. Figure 4 shows waveform shapes with the post-tap enabled and the pre-tap enabled respectively. Waveform linearity is well maintained even when the pre-emphasis taps are enabled, resulting in in superior signal integrity and a more stable stressed eye generated.

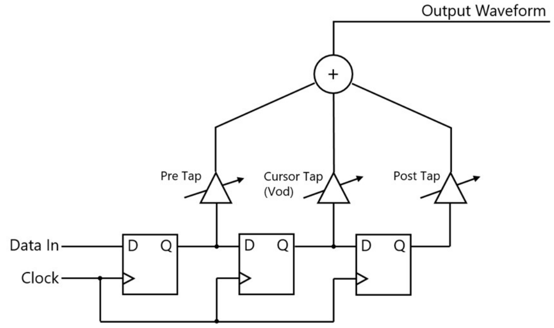
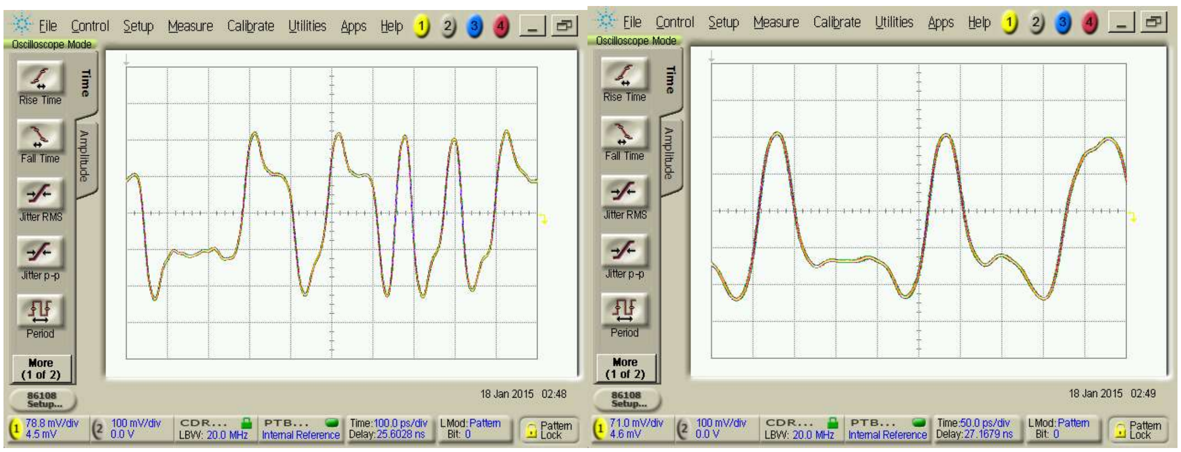


Figure 3. Illustration of pre-emphasis design



(a) (b)

Figure 4. Sample waveforms generated by the SV2C SerDes tester using the (a) post-tap and (b) pre-tap controls captured on an oscilloscope

Per-Lane Clock Recovery and Unique Dual-Path Architecture

In the SV2C, each receiver has its own embedded analog clock recovery circuit. Additionally, the clock recovery is monolithically integrated directly inside the receiver's high-speed sampler, thus offering the lowest possible sampling latency in a test and measurement instrument. The monolithic nature of the SV2C clock recovery helps achieve wide tracking bandwidth for measuring BER on signals that possess very high wander. Figure 5 shows a block diagram of the clock recovery capability inside the SV2C SerDes Tester.

Illustrated in Figure 5 is the per-lane adaptive equalization design. This design is based on a continuous-time linear equalizer (CTLE), offering DC gain, broad-band gain, and high frequency gain. Such architecture allows for correcting a wide range of transmission line losses. The CTLE can be programmed to perform automatic tuning based on the test environment and the incoming data payload.

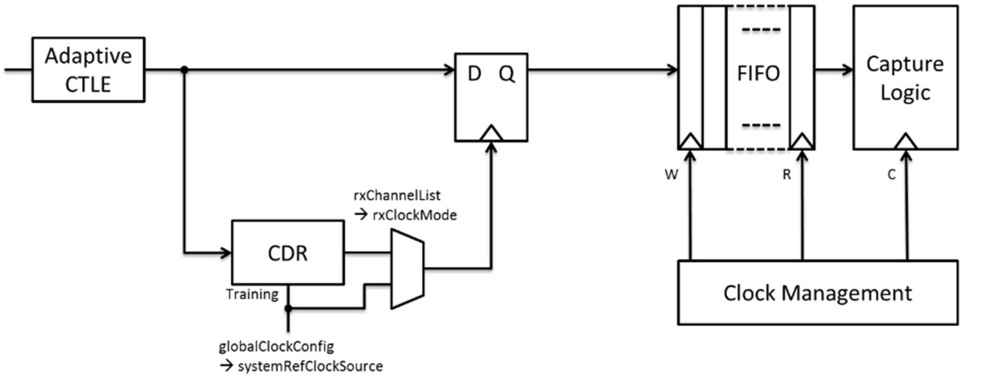
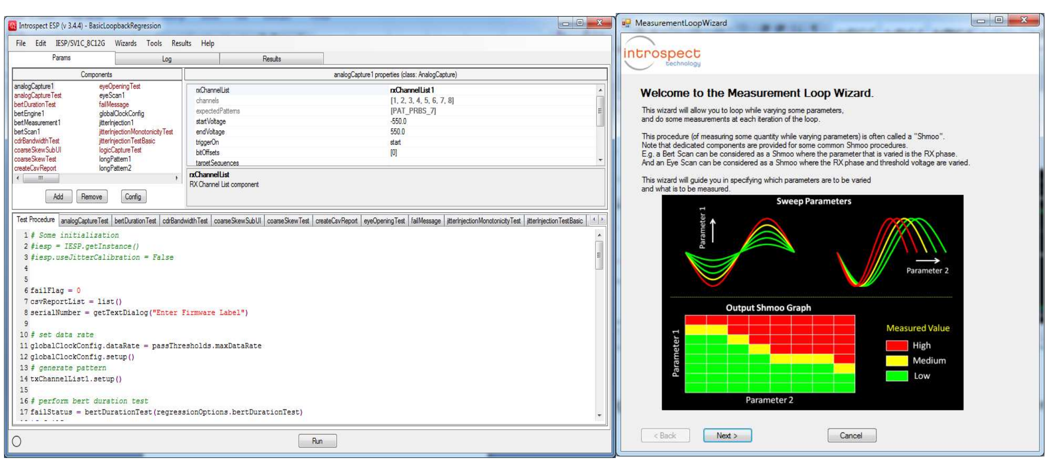


Figure 5. Per-lane clock recovery and CTLE architecture

Automation

The SV2C is operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 6(a). Component-based design is Introspect ESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the software environment features automatic code generation for common tasks such as the Measurement Loop Wizard as shown in Figure 6(b).



(a) *(b)*

Figure 6. Screen capture of IntrospectESP Software user interface (a) and its Measurement Loop Wizard (b)

Analysis

The SV2C features an independent bit error rate tester (BERT) on each of its eight high-speed receiver channels. Each BERT compares recovered and retimed data against a specified data pattern, and reports the accumulated bit error count. Included are built-in clock, 5th, 7th, 9th… 31st -order PRBS patterns, and user-defined patterns can be used as well.

BertScan, Figure 7, and eyeScan, Figure 8, enable fast, deterministic measurements of jitter, eye center, width and height and built-in and custom masks make automated pass/fail testing simple. Any time a measurement is executed the resulting raw data, plots, images and test procedures are automatically stored for easy recall.

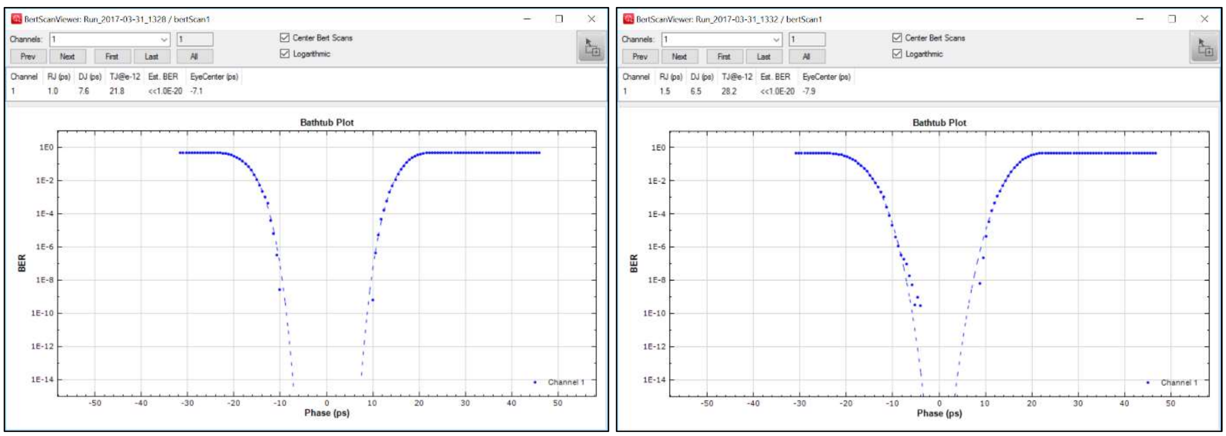


Figure 7. Example BERT Scan results of the SV2C at 26 Gbps, PRBS13 pattern and no impairments applied (left) and 0.9 UI random jitter injected (right)

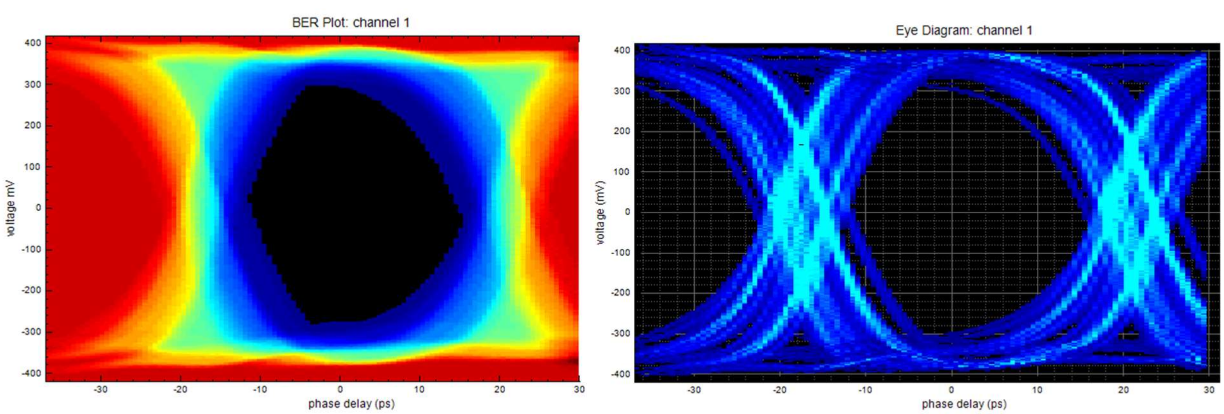


Figure 8. Example Eye Scan results of the SV2C at 26 Gbps, PRBS7 pattern displayed as a BER plot (left) and an eye diagram (right).

Simultaneous Parallel Loopback

The SV2C is the only bench-top tool that offers instrument-grade loopback capability on all differential lanes. The loopback capability of the SV2C includes:

- Retiming of data for the purpose of decoupling DUT receiver performance from DUT transmitter performance
- Arbitrary jitter or voltage swing control on loopback data

Figure 9 shows two common loopback configurations that can be used with the SV2C. In the first configuration, a single DUT's transmitter and receiver channels are connected together through the SV2C. In the second configuration, arbitrary pattern testing can be performed on an end-to-end communications link. The SV2C is used to pass data through from a traffic generator (such as an end-point on a real system board) to the DUT while stressing the DUT receiver with jitter, skew, or voltage swing.

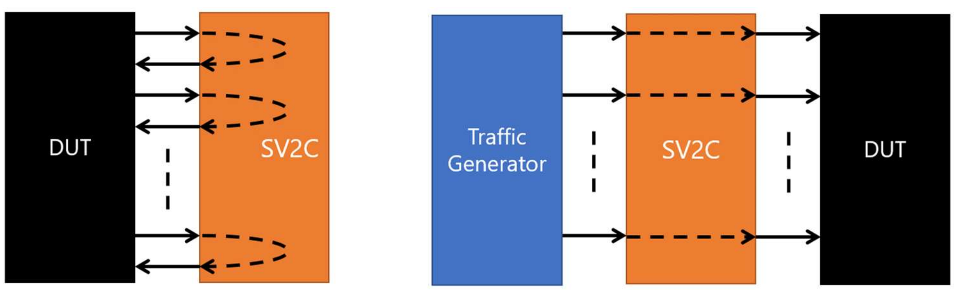


Figure 9. Illustration of loopback applications

Physical Description

The SV2C, shown in Figure 10, features two, 16-pin high-density connectors which deliver, and receive, high-speed data signals. Table 1 describes all available connections. Tables 2 and 3 describe the mapping of the Transmit and Receive Channels from their definitions in the Introspect ESP GUI to their physical pins on the front of the tester. Two differential clock outputs and one input are accessible by SMP connections for synchronizing the SV2C to a device under test.

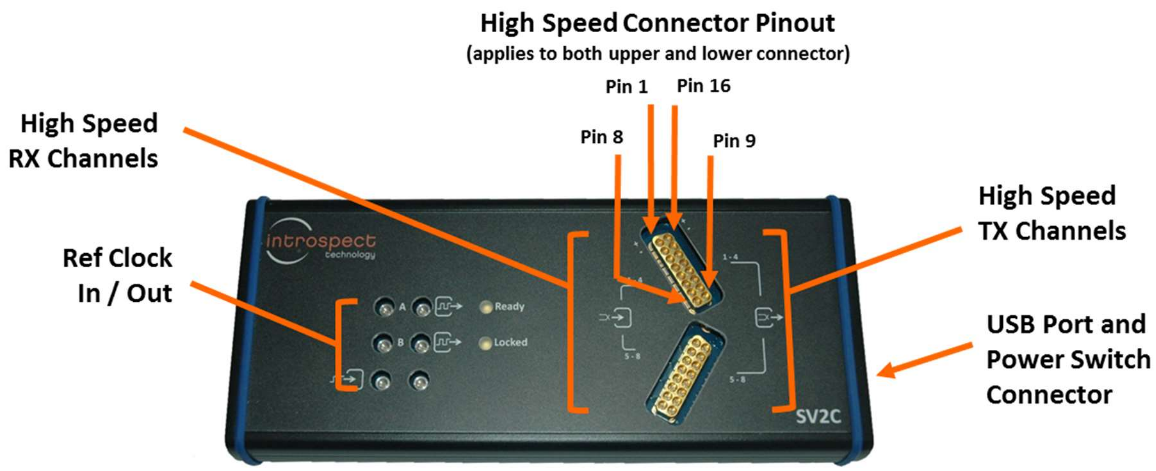


Figure 10. The Introspect SV2C Personal SerDes Tester

Table 1. Connector types of SV2C Personal SerDes Tester

Port / Indicator Name	Connector Type
Clock In	SMP Differential Pair
Clock Out A	SMP Differential Pair
Clock Out B	SMP Differential Pair
Ready Status LED	-
PLL Lock Status LED	-
Power Switch / Connector	-
USB Port	USB
Tx Channels 1-8	MXP
Rx Channels 1-8	MXP

Table 2. Receiver Channels Pin Mapping

Rx Channel	Connector, Pin Number
Ch 1 P/N	Upper, 1 / 2
Ch 2 P/N	Upper, 3 / 4
Ch 3 P/N	Upper, 5 / 6
Ch 4 P/N	Upper, 7 / 8
Ch 5 P/N	Lower, 1 / 2
Ch 6 P/N	Lower, 3 / 4
Ch 8 P/N	Lower, 5 / 6
Ch 9 P/N	Lower, 7 / 8

Table 3. Transmitter Channels Pin Mapping

Tx Channel	Connector, Pin Number
Ch 1 P/N	Upper, 16 / 15
Ch 2 P/N	Upper, 14 / 13
Ch 3 P/N	Upper, 12 / 11
Ch 4 P/N	Upper, 10 / 9
Ch 5 P/N	Lower, 16 / 15
Ch 6 P/N	Lower, 14 / 13
Ch 8 P/N	Lower, 12 / 11
Ch 9 P/N	Lower, 10 / 9

Specifications

Table 4. General Specifications

Parameter	Value	Units	Description and Conditions
Ports			
Number of Differential Transmitters	8		
Number of Differential Receivers	8		
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input.
Data Rates and Frequencies			
Programmable Data Rates	1 - 32	Gbps	Contact factory for extension to data rates.
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)

Table 5. Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
Output Coupling			
DC common mode voltage	1.2V – V_{OD}/2	mV	V_{OD} is programmed differential swing. Operate in AC coupled mode only.
AC Output Differential Impedance	100	Ohm	Typical
Voltage Performance			
Minimum Differential Voltage Swing	390	mV	
Maximum Differential Voltage Swing	1040	mVpp	
Number of Voltage Swing Steps	32		
Calibrated Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/- 10mV	%, mV	
Rise and Fall Time	15	ps	Typical, 20-80% (See Figure 12)
De-emphasis Performance			
Pre-Emphasis Pre-Tap Range	0 to 4	dB	High-pass function only, smallest range available based on worst-case conditions. Typical operating conditions result in wider range. Preliminary specific.
Pre-Emphasis Pre-Tap Resolution	Range / 20	dB	
Pre-Emphasis Post1-Tap Range	0 to 15	dB	High-pass function only, smallest range available based on worst-case conditions. Typical operating conditions result in wider range. Preliminary specific.
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	
Jitter Performance			
Random Jitter Noise Floor	700	fs	Preliminary specification. Measurement with DCA-X with 86108B Precision Waveform Analyzer.

Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	60	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1100	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Common		Common across all channels within a unit.
Maximum RMS Random Jitter Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	
Accuracy of Injected Jitter Magnitude	TBD	%, ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	TBD	ps	

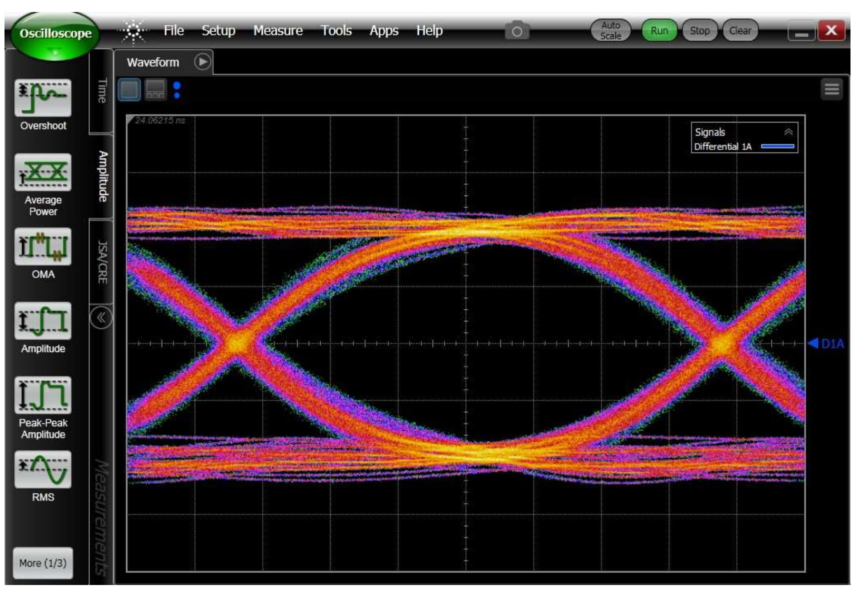


Figure 11. PRBS9 eye diagram at 28 Gbps

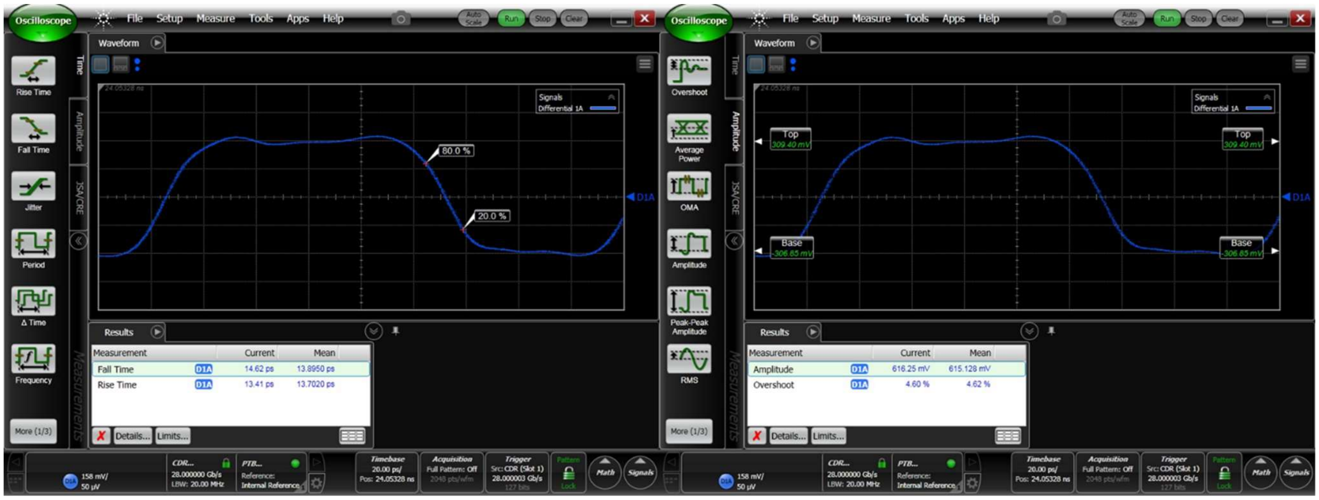


Figure 12. Typical signal waveform parameters.

Table 6. Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
AC Input Differential Impedance	100	Ohm	
AC Performance			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Differential Comparator Threshold Voltage Accuracy	TBD	%, mV	
Resolution Enhancement & Equalization			
DC Gain, CTLE Gain	Automatic	dB	DC Gain and CTLE Equalization can be set to automatic optimization or can be disabled.
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		

Table 7. Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	1		
Embedded Clock Applications			
Transmit Timing Modes	System Extracted		Clock can be extracted from one of the data receiver channels in order to drive all transmitter channels.
Receive Timing Modes	System Extracted		All channels have clock recovery for extracted mode operation.
Per-Lane CDR Tracking Bandwidth	Lane Rate / 1667		

Table 8. Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Loopback			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	Maintained across cascaded modules.
Preset Patterns			
Standard Built-In Patterns	All Zeros D21.5 K28.5 K28.7 DIV.16 DIV.20 DIV.40 DIV.50 PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.21 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
User-programmable Pattern Memory			
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	1024	bits	
Maximum Pattern Segment Size	131072	bits	
Total Memory Space for Transmitters	1	Mbits	Memory allocation is customizable. Contact factory.
Total Expected Memory Space for Receivers	1	Mbits	Memory allocation is customizable. Contact factory.
Pattern Sequencing			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	4		This refers to the number of sequencer slots that can operate at any given time. The instrument has storage space for 16 different sequencer programs.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
Additional Pattern Characteristics			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	

Table 9. Measurement and Throughput Characteristics

Parameter		Value	Units	Description and Conditions
BERT Sync				
	Alignment Modes	Pattern PRBS		Module can align to any user pattern or preset pattern.
	Minimum SYNC Error Threshold	3	bits	
	Maximum SYNC Error Threshold	2^{32}-1	bits	
	Minimum SYNC Sample Count	1024	bits	
	Maximum SYNC Sample Count	2^{32}	bits	
	SYNC Time	20	ms	Assumes a PRBS7 pattern that is stored in a user pattern segment and worst case misalignment between DUT pattern and expected pattern; data rate is 3.25 Gbps.
BERT				
	Error Counter Size	32	bits	Sample counts in the BERT are programmed in increments of 32 bits.
	Maximum Single-Shot Duration	2^{32}-1	bits	Repeat mode is available to continuously count over longer durations.
	Continuous Duration	Indefinite		
Alignment				
	CDR Lock Time	5	us	
	Self-Alignment Time	50	ms	

Table 10. Instruction Sequence Cache

Parameter		Value	Units	Description and Conditions
Simple Instruction Cache				
	Instruction Learn mode Instruction	Start Stop Replay		
Advanced Instruction Cache				
	Local Instruction Storage	1M Instructions		
	Instruction Sequence Segments	1000		

Revision Number	History	Date
1.0	Document release	Jan 20, 2016
1.1	Spec update	April 21, 2016
1.2	Spec update	May 5, 2017
1.3	Spec update	November 20, 2018

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