DATA SHEET

SV2C-PAM4

Personalized SerDes Tester

C SERIES

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MK-D032E-E-22259

INTROSPECT.CA

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Introduction

OVERVIEW

The SV2C-PAM4 is a highly integrated 58 Gbps (29 Gbaud) parallel tester that meets the emerging test requirements for 400 Gbe and CEI-56G connectivity applications. Featuring eight independent receivers and eight independent transmitters, the SV2C-PAM4 offers a truly flexible, high-volume, low-cost solution for the test and validation of next generation networking interfaces.

KEY BENEFITS

- True parallel bit-error-rate measurement across 8 lanes
- Programmable data rate selection from 39.2 Gbps – 58 Gbps
- Programmable output voltage on all transmitter lanes for receiver stress test applications
- Fully synthesized integrated jitter injection on all transmitter lanes
- Two-tap pre-emphasis control on all transmitter lanes
- Hardware clock recovery per lane
- Flexible loopback support per lane
- Support for both PAM4 and NRZ data patterns
- State of the art programming environment based on the highly intuitive Python language

APPLICATIONS

- CDR and transceiver production testing
- Parallel PHY validation of serial bus standards
- Parallel PHY validation and eye margining
- Interface tests of electrical/optical media
- Passive device testing

PHYSICAL CONNECTIONS

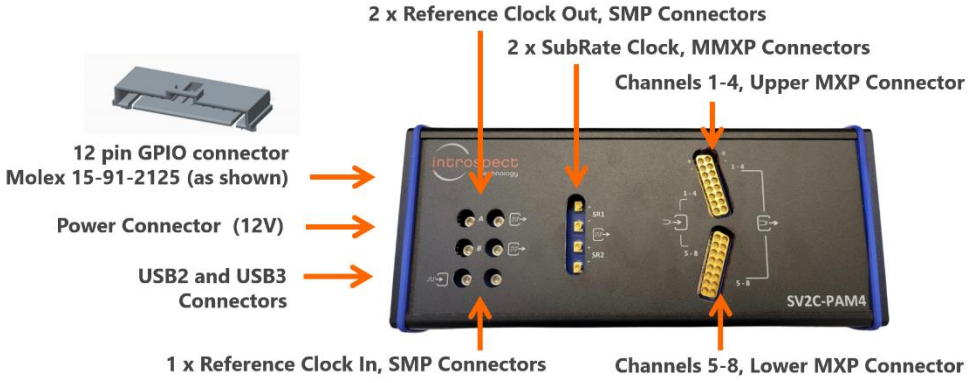
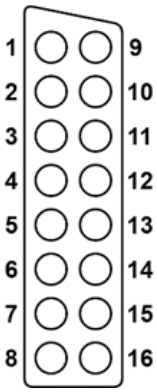


Figure 1: SV2C-PAM4 physical connections

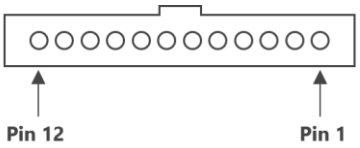
MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: SIGNAL MAPPING OF THE MXP CONNECTOR FOR SV2C-PAM4

	MXP PIN	UPPER MXP CONECTOR	LOWER MXP CONNECTOR
MXP Top View 	1	RX Channel 1 P	RX Channel 5 P
	2	RX Channel 1 N	RX Channel 5 N
	3	RX Channel 2 P	RX Channel 6 P
	4	RX Channel 2 N	RX Channel 6 N
	5	RX Channel 3 P	RX Channel 7 P
	6	RX Channel 3 N	RX Channel 7 N
	7	RX Channel 4 P	RX Channel 8 P
	8	RX Channel 4 N	RX Channel 8 N
	9	TX Channel 1 P	TX Channel 5 P
	10	TX Channel 1 N	TX Channel 5 N
	11	TX Channel 2 P	TX Channel 6 P
	12	TX Channel 2 N	TX Channel 6 N
	13	TX Channel 3 P	TX Channel 7 P
	14	TX Channel 3 N	TX Channel 7 N
	15	TX Channel 4 P	TX Channel 8 P
	16	TX Channel 4 N	TX Channel 8 N

LOW SPEED GPIO CONNECTOR PINOUT

TABLE 2: GPIO CONNECTOR PINOUT

CONNECTOR	PIN	INPUT/OUTPUT	FUNCTION
12 pin GPIO connector Molex 15-91-2125  A weak internal pull-up is present on all pins except ground. All pins use 1.8 V LVCMOS logic.	1	Configurable	GPIO[0]
	2	Configurable	GPIO[1]
	6	Configurable	GPIO[2]
	7	Configurable	GPIO[3]
	8	Configurable	GPIO[4]
	9	Configurable	GPIO[5]
	10	Configurable	GPIO[6]
	11	Configurable	GPIO[7]
	12	-	Ground

ORDERING INFORMATION

TABLE 3: ITEM NUMBERS FOR THE SV2C-PAM4 AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5158	SV2C-PAM4	58 Gbps, 8 Channel parallel PAM4 tester with Introspect ESP Software license
5258	SV2C-PAM4	58 Gbps, 8 Channel parallel PAM4 tester, instrument only

Features

FLEXIBLE OPERATING MODES

The SV2C-PAM4 contains multiple pattern generators and error detectors that can be operated independently. This allows the SV2C-PAM4 to be used in multiple applications without requiring any special hardware changes. The following example modes are supported:

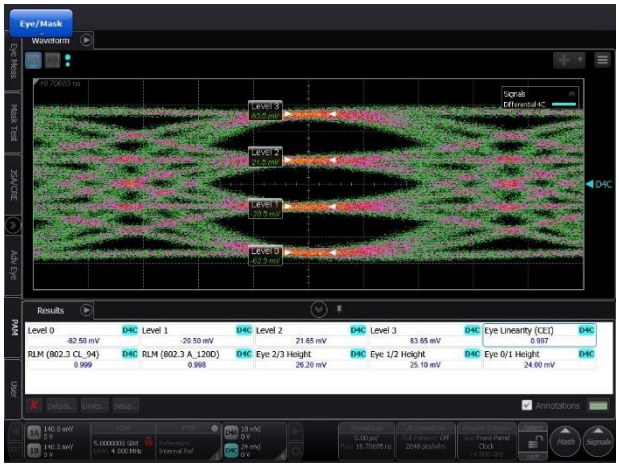
- Transmit only: the SV2C-PAM4 is used to drive test patterns and stressed eyes into a device under test (DUT) receiver and error checking happens inside the receiver
- Receive only: the SV2C-PAM4 is used as an error detector, measuring bit error rate from a DUT transmitter and analyzing eye height, linearity and jitter parameters
- Device loopback: the SV2C-PAM4 is used to drive test patterns and stressed eyes into a DUT receiver, and the same SV2C-PAM4 is used to receive patterns from the DUT transmitter to measure bit error rate, eye height, linearity, and jitter parameters
- Pass-through: the SV2C-PAM4 is used to receive arbitrary data from a transmitting DUT and then pass the data through to a receiving DUT while adding jitter or stressed eye impairments

PROGRAMMABLE OUTPUT VOLTAGE

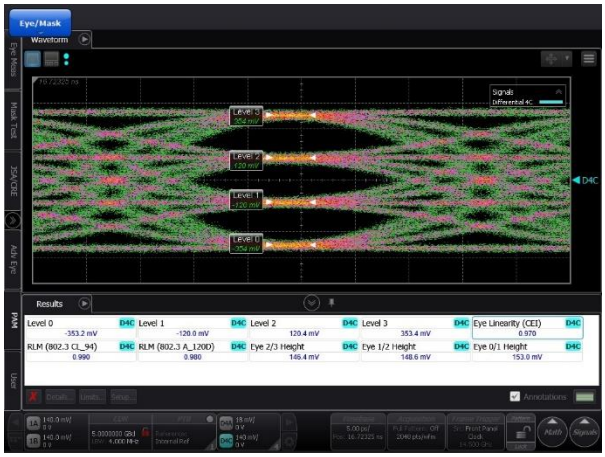
The SV2C-PAM4 allows programmable amplitude on a per-lane basis for both PAM4 and NRZ signal levels. Output amplitude may be programmed from 110 mVpp differential to 700 mVpp differential, each with a typical rise time of 13 ps. Example PAM4 signals for minimum and maximum voltage levels are shown in Figure 2 on the following page.

JITTER AND SKEW INJECTION

Like other products from Introspect Technology, the SV2C-PAM4 contains a full suite of internally synthesized jitter injection sources. Additionally, the SV2C-PAM4 can create PAM4-specific impairments such as signal distortion and amplitude level errors. Examples of sinusoidal jitter injection at 1 MHz, 2000 ps and 45 MHz, 25 ps are shown in Figure 3 on the following page. The time interval error (TIE) waveforms in the figure demonstrate the purity of the sine wave produced.



(a) 120 mVpp differential setting, 58 Gbps



(b) 700 mVpp differential setting, 58 Gbps

Figure 2: SV4E-PAM4 transmitter eye diagrams at (a) 120 mVpp and (b) 700 mVpp differential voltage settings

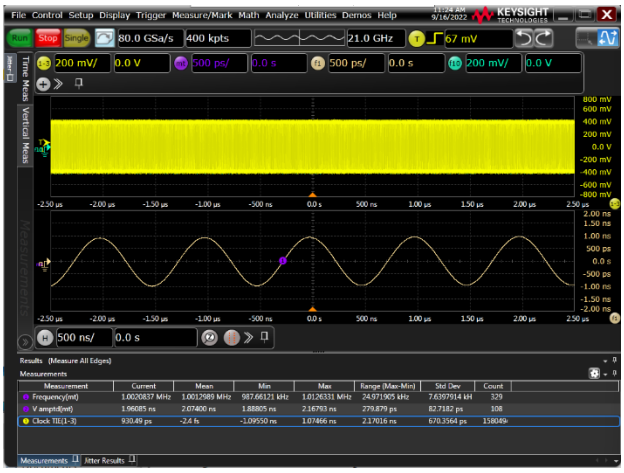


Figure 3: SV2C-PAM4 transmitter jitter injection examples (shown by TIE waveform) for (a) 1 MHz, 2000 ps sinusoidal jitter injection and (b) 45 MHz, 25 ps sinusoidal jitter injection

TRANSMIT AND RECEIVE EQUALIZATION

Each channel in the SV2C-PAM4 contains both transmit and receive equalization circuitry for optimizing signal performance across long channels. The transmitters incorporate pre- and post-tap de-emphasis. Similarly, the receivers incorporate both continuous-time linear equalization (CTLE) and decision-feedback equalization (DFE). Various adaptation algorithms are available for selecting optimal transmit and receive equalization values.

PER-LANE CLOCK RECOVERY

Each receiver in the SV2C-PAM4 contains a fully integrated clock and data recovery (CDR) circuit. This helps create a self-contained solution for production testing applications. It also ensures high performance eye tracking without suffering from long path delays like those found in legacy sampling oscilloscopes.

EYE MARGINING / VERTICAL EYE MEASUREMENT

The per-lane CDR mentioned above accurately places the receiver sampling point at the center of each received eye and enables precise voltage and linearity measurement for each lane. An example of a vertical eye measurement, including extrapolated vertical eye openings as viewed in the Introspect ESP Software tools, is shown in Figure 4. Measured and extrapolated values are listed along the right side of the figure, which include voltage levels, eye openings and linearity measurements. These parameters are directly accessible in Python code to facilitate production test automation.

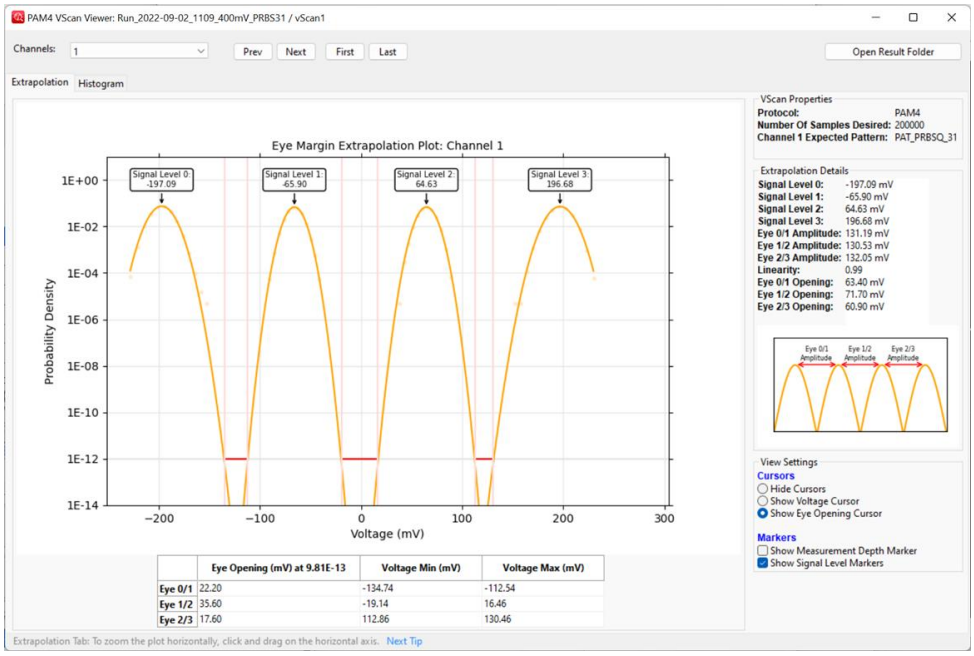


Figure 4: SV2C-PAM4 receiver measurement of vertical eye opening and linearity as viewed in the Introspect ESP Software

AUTOMATION

The SV2C-PAM4 is operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design. Based on the Python programming language, the Introspect ESP Software is able to interoperate with many external automation environments such as:

- Python: all Introspect ESP Software classes can be called from standard Python interpreters
- VBA: the Introspect ESP Software has utilities for integration with existing VBA automation examples
- C# and C++: Introspect Technology offers DLL for controlling the SV2C-PAM4 from within Windows applications developed in C# or C++
- LabView: using Python plug-ins, the Introspect ESP Software can be called from graphical programming environments such as LabView

Specifications

TABLE 4: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of Differential Transmitters	8		Can operate in NRZ or PAM4 mode
Number of Differential Receivers	8		Can operate in NRZ or PAM4 mode
Number of Sub-Rate Clock Outputs	2		Set frequencies at baud rate divided by a programmable integer value
Number of Dedicated Low Frequency Clock Outputs	2		
Number of Dedicated Low Frequency Clock Inputs	1		
Number of Programmable GPIOs	8		Can be set as trigger outputs based on events in the error detector logic
Data Rates and Frequencies			
Minimum Programmable Data Rate	39.2	Gbps	19.6 Gbaud
Maximum Programmable Data Rate	58	Gbps	29 Gbaud
Frequency Resolution of Programmed Data Rate	10	kbps	
Data Rate Absolute Accuracy	< 10	ppm	
Minimum External Reference Clock Input Frequency	10	MHz	
Maximum External Reference Clock Input Frequency	250	MHz	
Minimum External Reference Clock Output Frequency	10	MHz	
Maximum External Reference Clock Output Frequency	250	MHz	

TABLE 5: TRANSMITTER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Output Coupling			
Coupling Mode	DC		
Common Mode Voltage	500	mV	
AC Output Differential Impedance	100	Ohms	
Output Return Loss at 10 GHz	-15	dB	
Voltage Performance			
Minimum Differential Voltage Swing	110	mVpp	
Maximum Differential Voltage Swing	700	mVpp	
Resolution of Differential Voltage Setting	10	mV	
Voltage Swing Accuracy	±10	%, mV	Larger of 10% or 10 mV
Rise and Fall Time	13	ps	Typical, 20% - 80% value
De-Emphasis Performance			
Pre-Tap Range	8	dB	
Pre-Tap Resolution	17	steps	
Post-Tap Range	8	dB	
Post-Tap Resolution	17	steps	
Jitter Performance			
Random Jitter Noise Floor	300	fs	Typical. Measurement with DCA-X with 86108B Precision Waveform Analyzer

TABLE 6: JITTER INJECTION SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Sinusoidal Jitter Injection			
Minimum Frequency	0.1	kHz	
Maximum Frequency	60	MHz	At maximum data rate, greater than 1 UI of jitter injection supported at jitter frequencies up to 45 MHz
Frequency Resolution	0.1	kHz	
Maximum Peak-to-Peak Injected SJ	3000	ps	3000 ps at 1 MHz 700 ps at 10 MHz
Magnitude Resolution of Peak-to-Peak Injected SJ	300	fs	
Independent SJ Injection sources	8		Each channel is independently controlled for jitter injection
Random Jitter Injection			
Maximum RMS RJ Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	
Independent RJ Injection sources	8		Each channel is independently controlled for jitter injection
Bounded Uncorrelated Jitter Injection			
BUJ injection support	Yes		Maximum BUJ injection level to be determined
Independent BUJ Injection sources	8		Each channel is independently controlled for jitter injection

TABLE 7: RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Coupling Mode	DC		
AC Input Differential Impedance	100	Ohms	
Input Return Loss at 10 GHz	-12	dB	
Voltage Performance			
Minimum Detectable Differential Input Voltage (V_{ID} min, PAM4)	70	mVpp	For 10^{-6} error rate at 58 Gbps
Maximum Differential Input Voltage (V_{ID} max, PAM4)	800	mVpp	
Maximum Differential ADC Voltage Step Size	15 10 7	mV mV mV	For 700 mV input signals For 400 mV input signals For 100 mV input signals
Resolution Enhancement			
DC Gain, CTLE Gain	Auto		DC Gain and CTLE Equalization can be set to automatic optimization or can be disabled
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Tolerated Insertion Loss at 14.5 GHz	12	dB	Preliminary value
Jitter Performance			
Random Jitter Noise Floor	350	fs	Preliminary
CDR Tracking Bandwidth	DR/1667	MHz	DR stands for data rate

TABLE 8: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Loopback			
Rx to Tx Loopback Capability	Per Channel		
Lane to Lane Latency Mismatch	0	UI	
Preset Patterns			
Standard Built-In Patterns	Various		Refer to the Introspect ESP Software
Pattern Encoding	NRZ, PAM4		
PRBS Polynomials	5 … 31		Refer to the Introspect ESP Software
PAM4 Specific Patterns	Supported		Specific Patterns: PRBS[5-31]Q PRQS[5-31] SSPR
Pattern Choice per Transmit Channel	Per Channel		
Pattern Choice per Receive Channel	Per Channel		
User Programmable Patterns			
Individual Drive Pattern	Per Channel		
Individual Expected Pattern	Per Channel		
Minimum Pattern Segment Size	512	Bits	Software automatically pads shorter patterns so that they reach 512 bits
Total Memory for Transmitters	1	Mbits	
Total Memory for Receivers	1	Mbits	
Pattern Sequencing			
Sequence Control	Loop Infinite		
	Loop on Count		
	Play to End		
Loop Count per Sequencer Slot	2^{16}	UI	

Revision Number	History	Date
0.8	Target specifications	November 11, 2019
0.9	Updated specifications; changed number of lanes to 8; updated product name	November 3, 2020
1.0	Updated specifications; document release	July 15, 2021
1.1	Updated specifications	September 12, 2021
1.2	Updated specifications and added Figure 2 to 4.	September 16, 2022

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