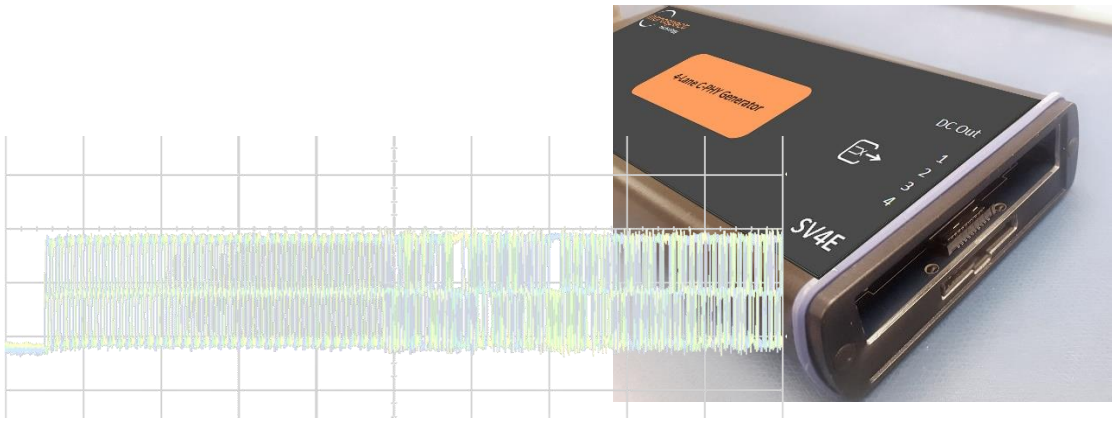
SV4E MIPI C-PHY/D-PHY DSI-2 Panel Tester



Data Sheet

Table of Contents

List of Figures

List of Tables

Introduction

Overview

The SV4E MIPI C-PHY/D-PHY DSI-2 Panel Tester is a highly versatile pattern generator suitable for turning on display panels and performing functional display test. It supports both C-PHY and D-PHY signalling interfaces, contains a large on-board memory, and provides an extremely flexible control interface.

Ideal for display panel testing and color calibration in a high-volume environment, the SV4E comes with an easy to use Control Panel and integrated Windows environment.

Key Benefits

- Complete DSI-2 support in a compact form factor
- Combo D-PHY and C-PHY signaling technology helps protect investment over multiple product generations
- Support for video-mode, command mode, tearing effect, and many advanced DSI-2 protocol requirements
- Support for compression algorithms based on the Vesa DSC standard

Applications

- Display Driver IC demonstration/evaluation board development
- Production testing of display panels
- Calibration and failure analysis
- Firmware and software integration and debug

Features

Block Diagram

The SV4E is a pattern-generator compliant with the most recent MIPI C-PHY specifications, including creation of low-power (LP) and high-speed (HS) protocol events. Figure 1 illustrates the block diagram and the architecture that allows unique control over LP and HS events, ensuring compliant DSI-2 packets and video frame transmission.

Built into the HS generators within the SV4E are the dedicated hardware C-PHY mapper and encoder. This allows for tremendous ease of use and true host-controller emulation, all from within a single, Windows-based software environment.

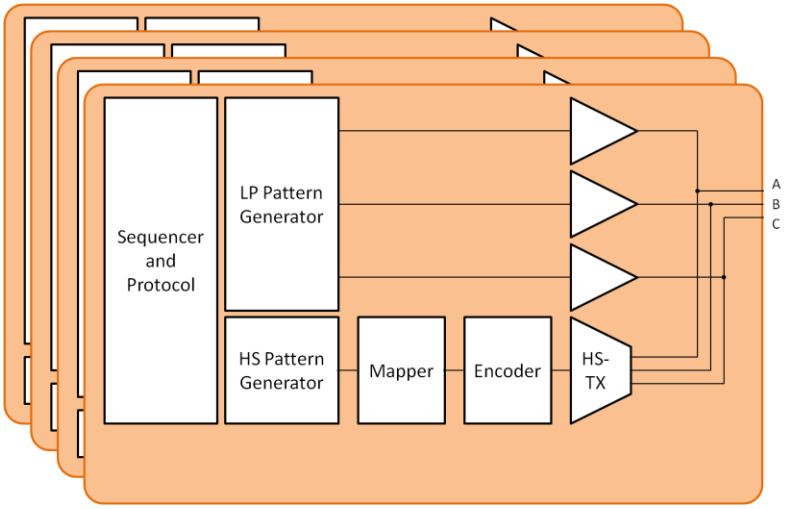


Figure 1 Block diagram of C-PHY generator inside SV4E

Simple User Interface

The SV4E is controlled using a PC from a Windows operating system. The software is amenable for production environments, minimizing operator involvement and maximizing throughput. Figure *2* shows the GUI where a single entry page is used to specify DSI parameters such as pixel format and transmission mode (video versus command). The figure also shows an example of a high-definition video sequence being produced by the SV4E, mimicking high frame rate video transmissions in either command-mode or video-mode.

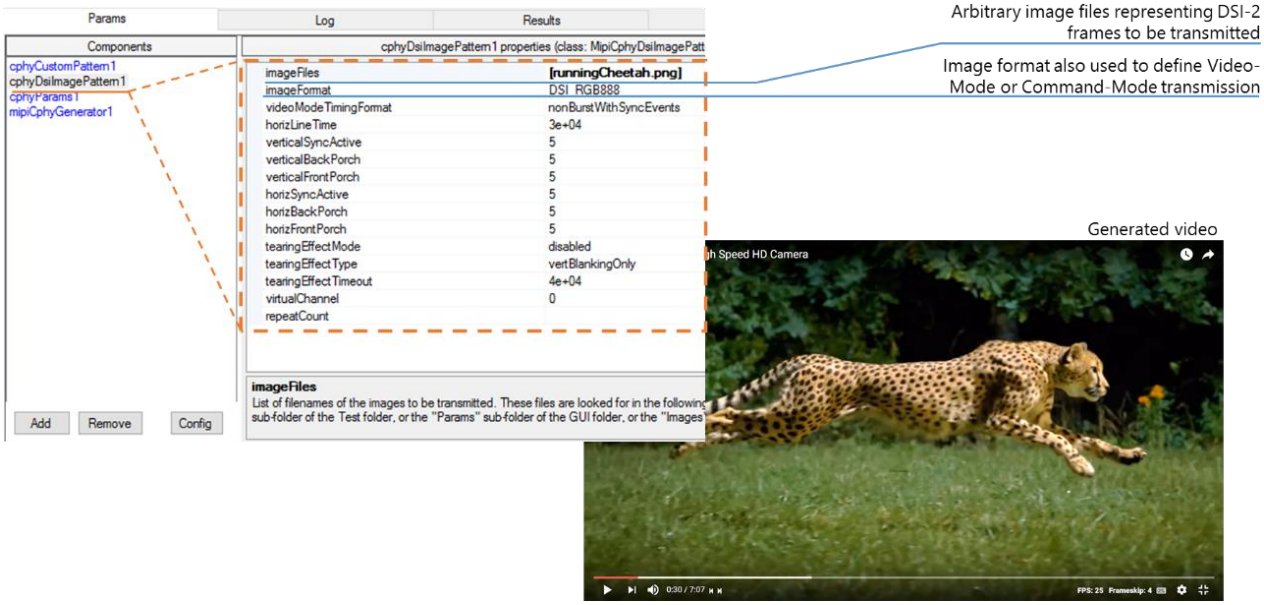


Figure 2 Illustration of the main software interface for generating DSI-2 traffic.

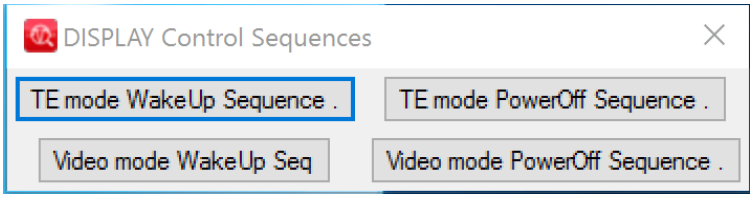


Figure 3 Simplified wake-up and power-down sequence controls.

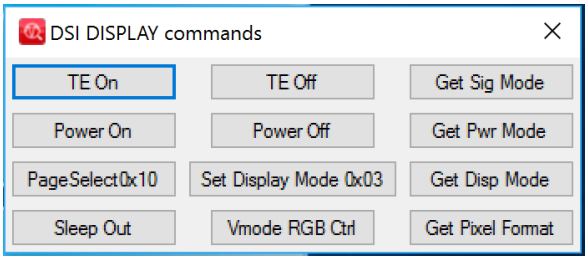


Figure 4 Individual DSI-2 panel commands useful for debug or failure analysis.

Apart from the simple automated setup, the software environment offers control panels for individually programming wakeup sequences or power down sequences as well as debugging single display commands, illustrated in Figure 3 and Figure 4.

Connection Diagrams

The SV4E offers a single low-cost connection scheme to display adapter modules, illustrated in Figure 5. The SV4E contains a Samtec QTH connector that carries both the C-PHY signals as well as low-speed control pins an auxiliary 5V DC output.

The SV4E mates to the display adapter module in a mezzanine configuration as illustrated in Figure 6. Note that the adapter board needs to extend away from the edge of the SV4E as shown in the drawing. Alternatively, Samtec-provided coaxial cables are available for further flexibility of attachment to display modules.

Figure 5 Photograph of SV4E tester showing Samtec QTH connector.

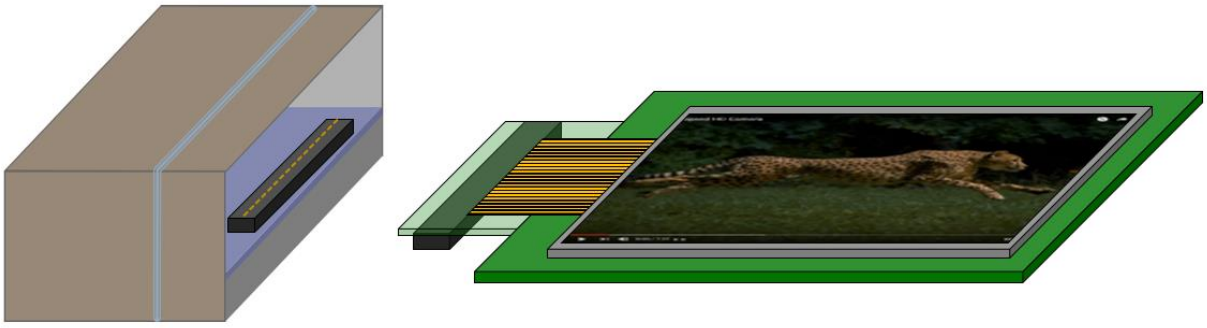


Figure 6 Illustration of Introspect SV4E, left, connecting to display adapter board, right, via Samtec connectors.

Specifications

Table 1 General Specifications

Parameter	Value	Units	Description and Conditions
Application / Protocol Support			
Physical layer interface	*C-PHY*		
MIPI protocol	*DSI-2*		*Flexible pattern architecture allows for the generation of encoded PHY data, unencoded PHY data, or entire DSI-2 protocol data* *Tester supports automatic acknowledge and error report readout from device receivers through the C-PHY BTA capability*
Compression protocol	*Vesa DSC v 1.11*		
Ports			
Number of Transmitter Trios	*2* *4*		*Order code SV4E-2* *Order code SV4E-4*
Number of GPIO Pins	*16*		*2.5 V LVCMOS I/O pins capable of executing pattern vectors*
Number of Flag Output Pins	*2*		*Additional configurable flag pins*
Auxiliary Output Supply Voltage	*5*	*V*	*Single supply voltage for powering peripheral devices such as a Display Adapter Board*
Data Rates and Frequencies			
Minimum Data Rate	*80*	*Msps*	
Maximum Data Rate	*1.5*	*Gsps*	*Contact factory for higher data rates*
Maximum GPIO Clock Frequency	*10*	*MHz*	

Table 2 Transmitter Characteristics

Parameter	*Value*	*Units*	*Description and Conditions*
HS Output Coupling			
Output Single-Ended Impedance	*50*	*Ω*	
Output Impedance Tolerance	*+ / - 5*	*Ω*	
HS Voltage Performance			
Minimum |VOD|	*0*	*mV*	
Maximum |VOD|	*250*	*mV*	
|VOD| Programming Resolution	*10*	*mV*	
Level Setting	*Per-Wire*		
LP Voltage Performance			
Minimum LP High Level	*700*	*mV*	
Maximum LP Low Level	*100*	*mV*	
Global Timing Parameters			*Timing parameters are programmable in the GUI*
t3-Prepare	*100*	*ns*	
ths-Exit	*300*	*ns*	
tLPX	*100*	*ns*	
tA-Go	*400*	*ns*	
t3-Prebegin	*196*	*UI*	
t3-ProgSeq	*14*	*UI*	
t3-Preend	*7*	*UI*	
t3-Post	*112*	*UI*	

Table 3 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	*1*		
Frequency Resolution of Programmed Data Rate	*1*	*Kbps*	

Table 4 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Preset Patterns			
Packet Loop	*PRBS*		*Repetitive PHY packets consisting of LP111 segments, a valid HS-entry sequence, and a payload consisting of PRBS data*
	Symbol Sequence		*Same as above, but with user-specified symbol sequences within the payload of the PHY packet*
	Integer Data		*Same as above, but with the payload specified in terms of 16 bit integers*
LP Only	*Infinite Loop*		*Repetitive transmission of user-specified LP states*
	One-Shot		*Single transmission of an LP sequence*
HS Only	*PRBS*		*A single HS-entry sequence is performed, followed by an infinite repetition of looping PRBS data*
	Symbol Sequence		*Same as above, but the looping data is based on user-specified symbol sequences*
	Integer Data		*Same as above, but the looping data is entered in terms of 16 bit integers*
DSI-2 Color Bar	*Command Mode*		
	Command Mode with Tearing Effect		
	Burst Mode		
	Non-Burst Mode with Sync Events		
	Non-Burst mode with Sync Pulses		
Arbitrary DSI-2 Patterns			
Lane Distribution	*TRUE*		*Allows duplication of generated patterns across the two trios or more for debug*
	FALSE		
Available Pattern Memory for Transmitters	*1*	*Gbits*	*Memory is used to house compiled C-PHY patterns consisting of integer data, LP data, and pattern sequencer programs*
Custom Pattern Sequencer			*Allows generation of arbitrary generic or DCS register commands*
Sequence Control	*Loop infinite*		
	Loop on count		*Count is a user defined number that is specified later in this section*
	Play to end		
Number of Sequencer Slots per Pattern Generator	*16*		*Each pattern generator can string up to 16 different segments together, each with its own repeat count. See illustration under Notes*
Number of Entry Slots	*1*		*See illustration under Notes*
Number of Exit Slots	*1*		*See illustration under Notes*
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		

Table 5 DUT Control Capabilities

Parameter	Value	Units	Description and Conditions
GPIO Port			
Data Drive Formats	*H*		*Using a text vector file, each pin can be programed to drive High, Low, or to go into high-impedance state*
	L		
	X		
Data Compare Formats	*H*		*Using a text vector file, each pin can compare against expected data*
	L		
	X		
Pattern Vector Length	*TBD*		

Table 6 Software Environment and Mechanical Dimensions

Parameter	Value	Units	Description and Conditions
OS Support			
Windows 7	*Yes*		
Windows 8	*Yes*		
Windows 10	*Yes*		
License Protection			
Node-Locked	*Yes*		
Communications Interface			
USB	*Yes*		
Dimensions			
Length	*6.5*	*inch*	
Width	*3.5*	*inch*	
Height	*1.5*	*inch*	
Display Connector			
Introspect SV4E			*Samtec QTH-040-XX-L-D-DP*
Display Adapter (not included)			*Samtec QSH-040-01-L-D-DP-A*

Revision Number	History	Date
1.0	Document creation	December 11, 2016
1.1	Minor text modifications; removed preliminary markings; updated specifications	March 29, 2017

The information in this document is subject to change without notice and should not be construed as a commitment by Introspect Technology. While reasonable precautions have been taken, Introspect Technology assumes no responsibility for any errors that may appear in this document.

Published on March 29, 2017
EN-D010E-E-17088