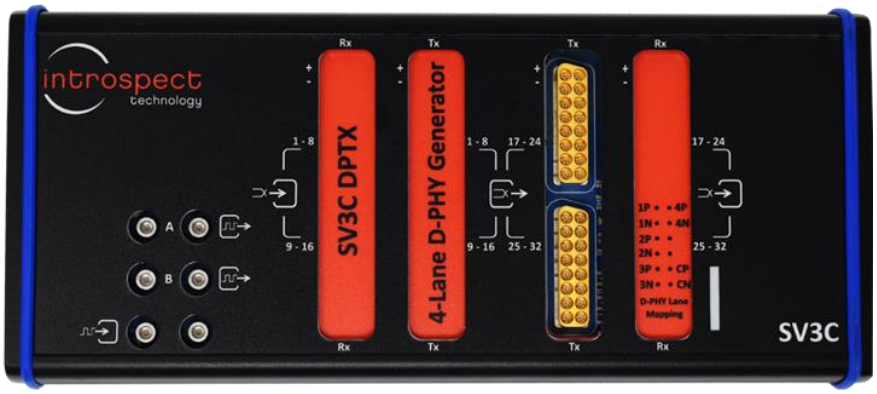
DATA SHEET

SV3C-DPTX

MIPI D-PHY Generator

C SERIES



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Introduction

OVERVIEW

The **SV3C-DPTX MIPI D-PHY Generator** is an ultra-portable, high-performance instrument that enables characterization and validation of MIPI D-PHY receiver ports. The instrument operates at up to 6.5 Gbps and includes analog parameter and precision timing controls that enable deep insights into receiver performance, including voltage and skew sensitivities and jitter tolerance.

The instrument operates with the easy-to-use, highly versatile Introspect ESP Software environment which includes a full suite of tools for generation of packets, test patterns, color bars and video frames for both CSI-2 and DSI-2. Introspect ESP software enables complete automation for MIPI D-PHY receiver testing and MIPI compliance test suites (CTS) are available.

KEY FEATURES

- D-PHY Physical Layer: four D-PHY lanes with integrated LP/HS signaling and support for a continuous range of data rates from 80 Mbps to 6.5 Gbps
- D-PHY Protocol Layer: fully supports CSI-2 and DSI-2-pixel formats, DSI-2 DSC and V-DCM decompression, and DSI-2 Display Command Sets (DCS)
- Voltage Controls: HS amplitude, HS common mode voltage, and LP voltage levels
- Timing Impairments: per-lane skew injection with < 1 ps resolution and per-lane multi-source jitter injection

KEY BENEFITS

- **Self-Contained**: an all-in-one system that enables the simplest bench environment for physical layer test to full protocol layer validation
- **Automated**: leverages the full power of Python and award-winning Introspect ESP Software Scripting capability is ideal for debug tasks and for full-fledged production screening of devices and systems
- **Future Proof**: protect your investment by adopting a high-performance tool for multiple product applications and across a large span of data rates

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV3C-DPTXCPTX AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
4584	DPTX D-PHY Generator	SV3C-DPTX with full impairment capability including jitter injection
4591	DPTX-APIX – Speed Upgrade Option for D-PHY	Speed upgrade option to 6.5 Gbps
4593	DPTX Upgrade to include C-PHY Generator Capability	Combination D-PHY and C-PHY generation capability
4595	CPTX-SPD1: Speed Upgrade Option for C-PHY	Speed upgrade option for C-PHY to 4.5 Gsps

Product Features

PHYSICAL DESCRIPTION AND PINOUT

Figure 1 shows a diagram of the physical ports of the SV3C-DPTX.

Figure 1: Illustration of the SV3C-DPTX MIPI D-PHY Generator system.

The SV3C-DPTX has two high-speed MXP connectors. The lower MXP connector, as shown in Figure 1, provides the differential TX lanes 1-4 and the differential clock output signal. The pin mapping for the lower connector is provided in Table 2. No-connect (NC) pins should not be used.

The upper MXP connector shown in Figure 1 provides three replica signals which may be connected directly to an external measurement device for live monitoring. The pin mapping for the upper connector is provided in Table 3.

TABLE 2: LOWER MXP CONNECTOR, LANE PINOUT

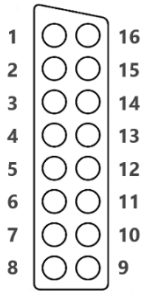
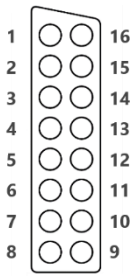
CONNECTOR	PIN	LANE
	1, 2	TX Lane 1 (P, N)
	3, 4	TX Lane 2 (P, N)
	5, 6	TX Lane 3 (P, N)
	16, 15	TX Lane 4 (P, N)
	12, 11	Clock Lane (P,N)
	7, 8, 9, 10, 13 and 14	NC

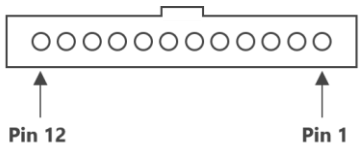
TABLE 3: UPPER MXP CONNECTOR, LANE PINOUT

CONNECTOR	PIN	LANE
	7	TX Lane 1 (P, replica)
	8	TX Lane 2 (N, replica)
	10	TX Lane 4 (P, replica)
	1 to 6, 9, 11 - 16	NC

The 12 pin connector on the left side of the module, as shown in Figure 1, provides access to six GPIO pins and a ground pin. The connector pinout is given in Table 4, and the Molex connector part number is shown in the same table. All GPIO pins are 2.5 V LVCMOS compatible.

Please see the "General Purpose I/O and I2C Bus" section later in this document for the description of the GPIO and pin functions.

TABLE 4: GPIO CONNECTOR PINOUT

CONNECTOR	PIN	INPUT/OUTPUT	INTERNAL PULLUP/ PULLDOWN RESISTORS	FUNCTION
12 pin GPIO connector Molex 15-91-2125  	1	Configurable	Weak Pull Up	GPIO[0] or Daisy Chain Trigger Out
	2	Configurable	Weak Pull Up	GPIO[1] or I2C_SCL
	3	Configurable	Weak Pull Up	GPIO[2] or I2C_SDA
	4	Configurable	Pull Down	GPIO[3]
	5	Configurable	Pull Down	GPIO[4]
	6	Input Only	Pull Down	Tearing Effect Input
	12	-	-	Ground

DATA RATE PERFORMANCE

The SV3C-DPTX data rate may be programmed over a continuous range from 80 Mbps to 6.5 Gbps. The SV3C-DPTX maintains calibrated clock/data alignment and programmed skews are applied over the entire data rate range.

INTEGRATED LP AND HS GENERATION

The SV3C-DPTX offers truly integrated LP pattern generation as illustrated in Figure 2(a) and (b). The inclusion of LP allows for the creation of realistic stimulus conditions, and it enables the validation of key MIPI D-PHY global timing parameters. Figure 2(b) illustrates an example of the voltage control of the SV3C-DPTX. Lane 1 in the figure has been programmed with a positive HS common voltage, while Lane 4 has been programmed with a negative common mode voltage.

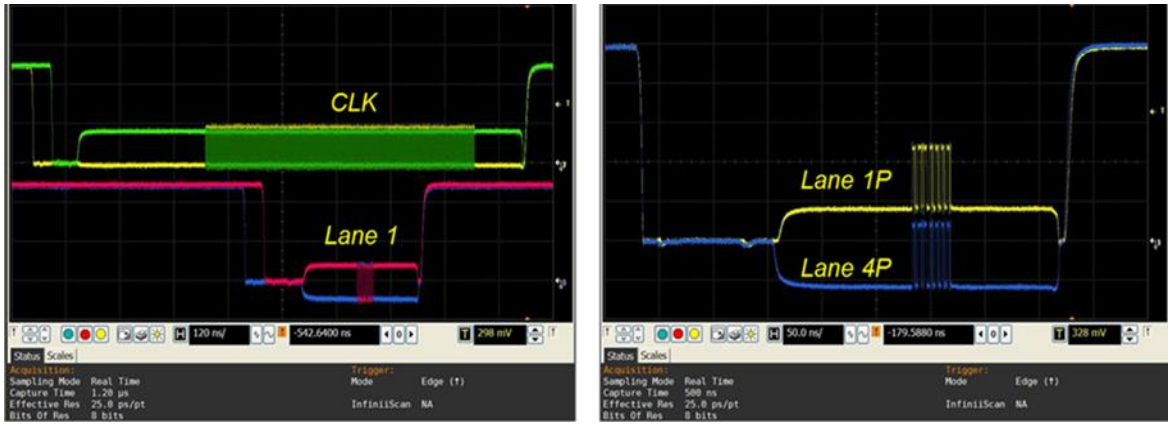


Figure 2: The left-hand figure shows the SV3C-DPTX waveform showing complete packet transmissions. The right-hand figure shows an example of voltage control.

HS TIMING CONTROLS

The SV3C-DPTX offers precise control over HS timing with skew adjustment resolution of 1 ps. Figure 3(a) illustrates a sample skew sweep which can be injected between HS clock and the data lines, and Figure 3(b) demonstrates the individual jitter injection control for each HS clock and data lane. In the figure, Lane 4 is programmed to inject higher jitter than Lane 1.

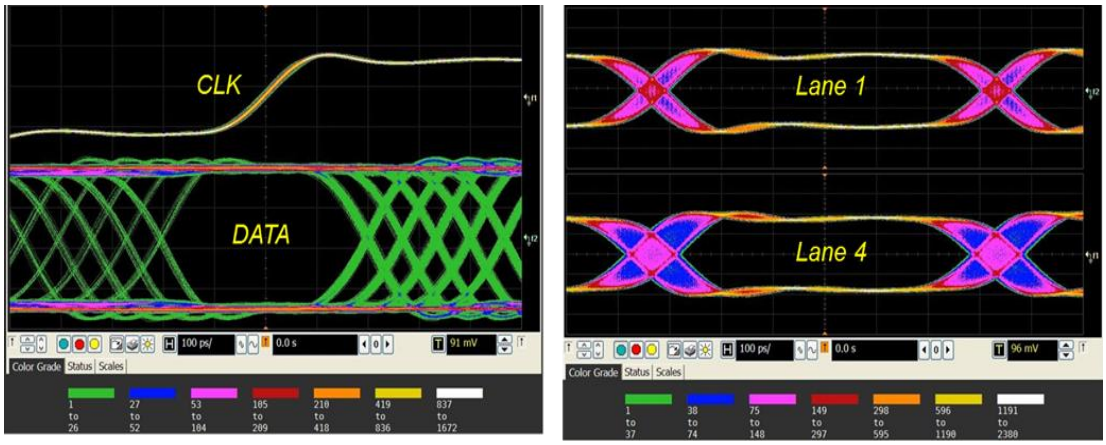


Figure 3: SV3C-DPTX generated waveforms demonstrating HS timing control. The left-hand figure shows an example of sweeping skew between CLK and DATA. The right-hand figure is an example of jitter injection.

COMPLETE PHYSICAL LAYER TESTING

For physical layer testing, the SV3C-DPTX generates highly configurable MIPI D-PHY stimulus signals and provides full control over key timing parameters associated with HS-entry and HS-exit transitions. A list of several key timing parameters controlled by the SV3C-DPTX is given in Table 5 on the following page. Typical waveforms are shown in Figure 4.

Please also refer to Figure 7 on page 11 for an example of the Introspect ESP software which shows the intuitive user interface for programming timing parameters.

TABLE 5: KEY MIPI TIMING PARAMETER AND BIT PATTERN CONTROLS

PARAMETER TYPE		TIMING PARAMETERS	PATTERN DEFINTIONS
HS Entry	Clock	$T_{CLK-LPX}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$	Start of Transmission (SoT) Clock zero bits
	Data	T_{LPX}, $T_{HS-PREPARE}$, $T_{HS-ZERO}$	Start of Transmission (SoT) HS zero bits
HS Exit	Clock	$T_{CLK-TRAIL}$, $T_{CLK-POST}$	Clock trail bits
	Data	$T_{HS-TRAIL}$, $T_{HS-EXIT}$	HS trail bits

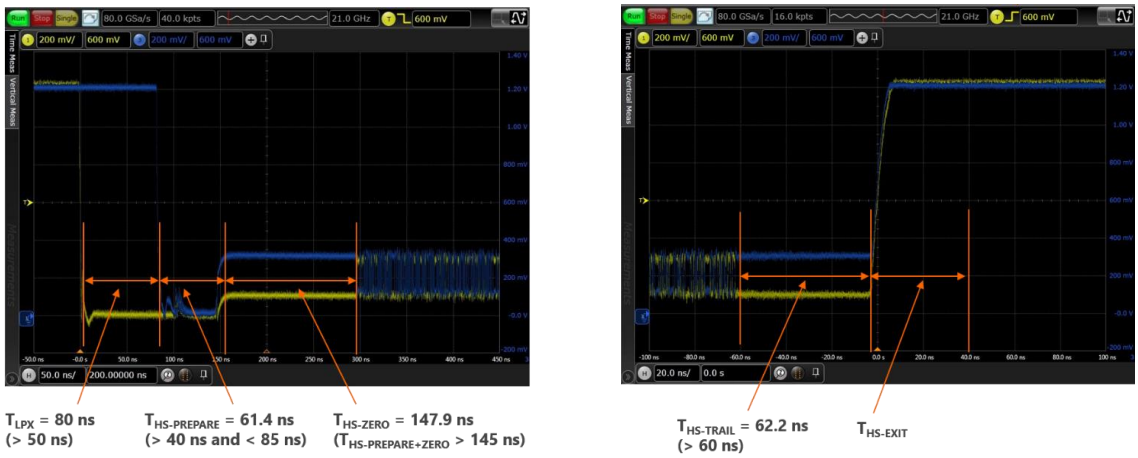


Figure 4: Waveforms showing key timing parameter controls available with the SV3C-DPTX.

PROTOCOL LAYER TESTING

For protocol testing, the Introspect software environment includes MIPI pattern tools that enable the generation of complete DSI-2 or CSI-2 packets, color bars and test patterns. All common pixel formats are supported. The SV3C-DPTX supports DSI-2 features such as the MIPI Display Command Set (DCS) as well as data compression formats (DSC and V-DCM). For further information on supported features refer to Table 12 in the "Specifications" section of this document.

INTROSPECT ESP SOFTWARE INTERFACE

The SV3C-DPTX is operated using award winning Introspect ESP Software. It features a comprehensive scripting language (Python) and an intuitive component-based design as shown in the screen shots in Figure 5 to Figure 7. Component-based design is Introspect ESP's way of flexibly organizing the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, allowing program development and execution in a matter of minutes.

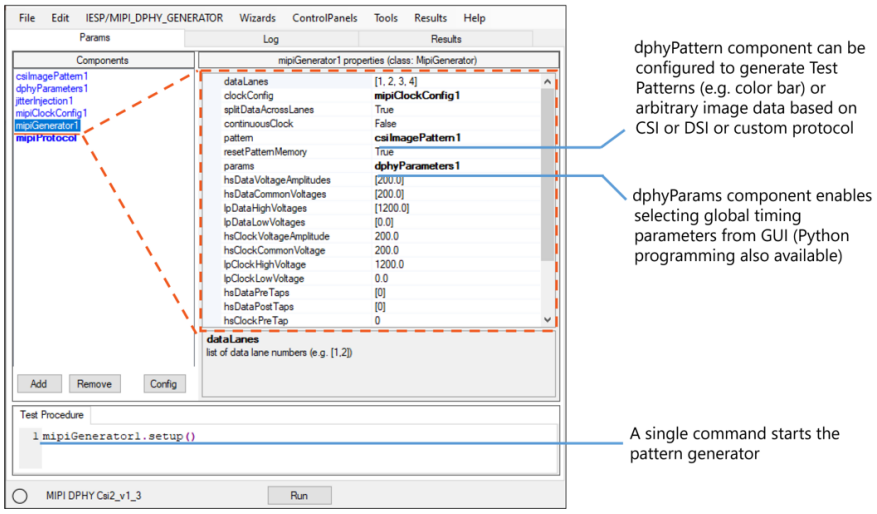


Figure 5: Illustration of the SV3C-DPTX software interface. The "MIPI generator" component and its properties are shown.

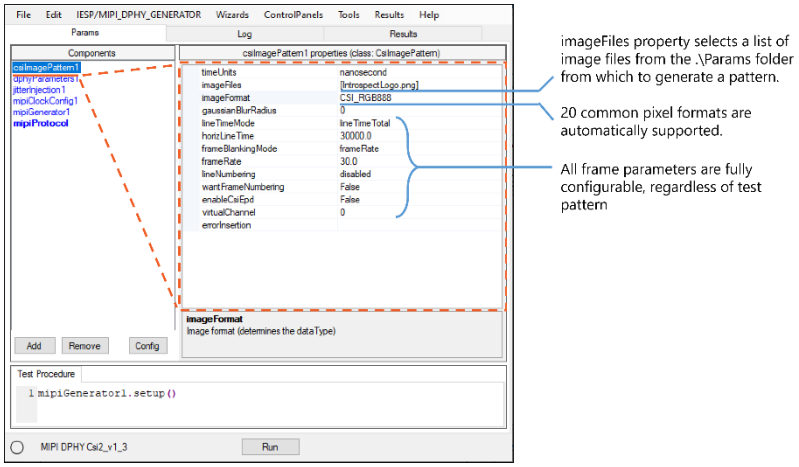


Figure 6: Illustration of the SV3C-DPTX software interface. The MIPI "CSI Image Pattern" component and properties are shown.

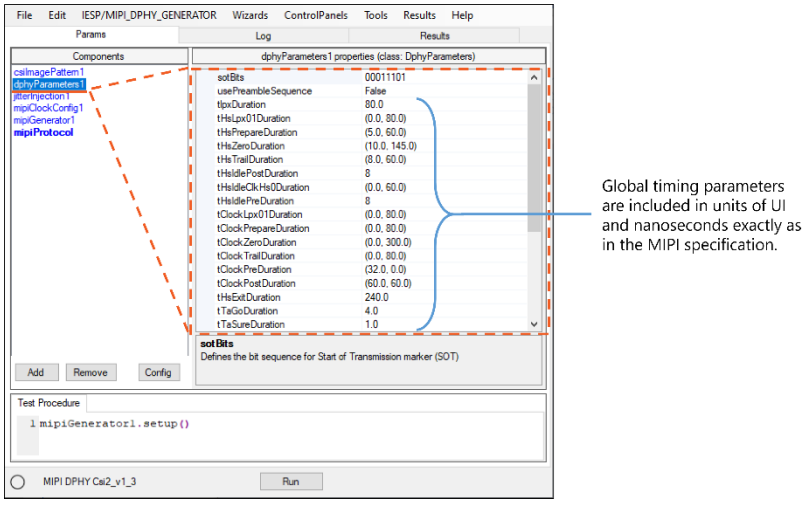


Figure 7: Illustration of the SV3C-DPTX software interface. The "DPHY Parameters" component and properties are shown.

MIPI COMPLIANCE TEST SUITES (CTS)

Introspect has implemented MIPI Compliance Test Suites within the Introspect ESP software environment. This includes test suites for both C-PHY and D-PHY, and for both transmitter and receiver compliance testing. A full list of CTS applications available for the SV3C-DPTX are provided in Table 6 below. An overview of the software interface and features of the D-PHY Receiver CTS Application, as implemented with the SV3C-DPTX MIPI D-PHY Generator, is shown in Figure 8.

Compliance test suites from Introspect provide convenient methods for selecting and executing tests, generate easy-to-read summaries of Pass/Fail compliance test results, and present clear individual summary reports for each compliance test executed. Each CTS application contains code which may be customized, particularly to allow for test automation. For example, custom code can facilitate the execution of external scripts using .NET DLLs to directly control devices under test (DUTs).

TABLE 6: MIPI CTS SUITES AVAILABLE FOR THE SV3C-DPTX

PART NUMBER	DESCRIPTION	MIPI SPECIFICATION DOCUMENT
5401	D-PHY Receiver CTS Application	mipi_D-PHY-v2-1_CTS_v1-0
5403	D-PHY CSI-2 Receiver CTS Application	mipi_CSI-2_v1-3_CTS_Receiver_v1-0 mipi_CSI-2_v2-1_CTS_Receiver_v1-0
5404	D-PHY DSI Receiver CTS Application	mipi_DSI-v1-3-1_CTS-Receiver_v1-0 *

* At the time of publication of this datasheet, mipi_DSI-v1-3-1_CTS-Receiver_v1-0 was the most recent official CTS release approved by MIPI. The DSI-2 CTS will be supported by Introspect once the DSI-2 CTS receives official MIPI board approval.

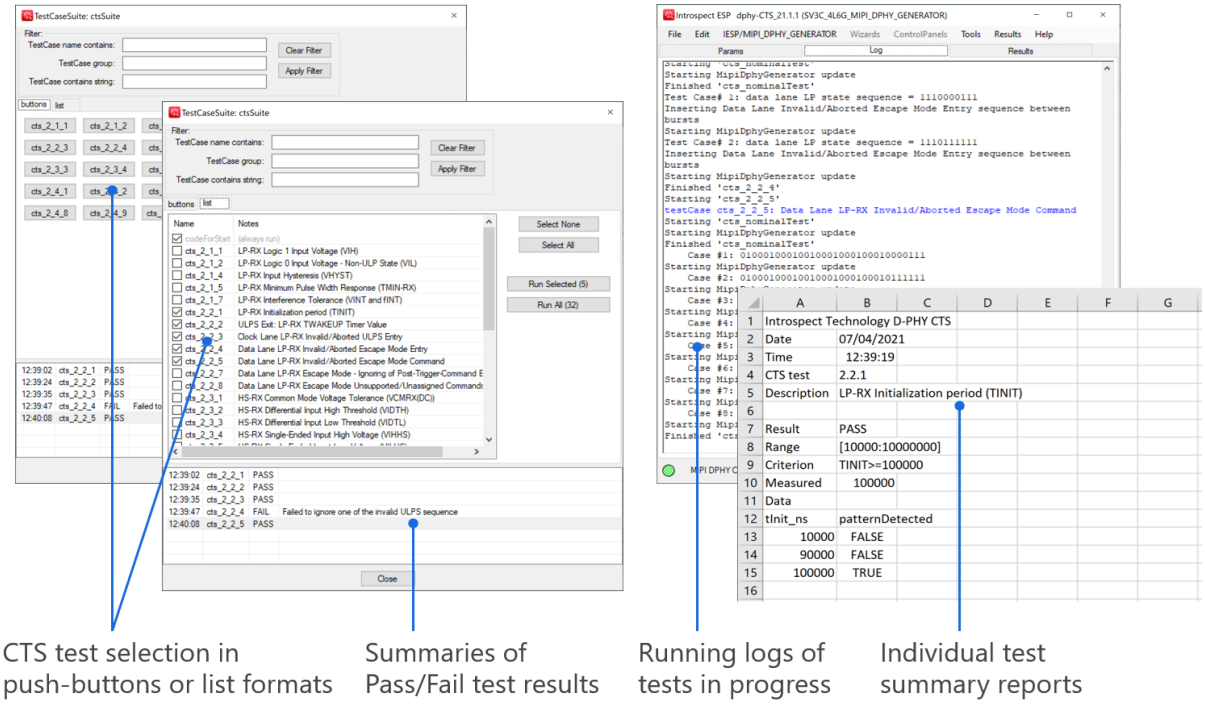


Figure 8: Example of the CTS software interface and features.

INPUT AND OUTPUT REFERENCE CLOCKS

The SV3C-DPTX allows for direct synchronization with an external input reference clock. The input reference frequency range is from 10 MHz to 250 MHz and the reference clock interface is compatible with 1.8 V to 3.3 V LVDS or LVPECL. The SV3C-DPTX also provides two external reference clocks. The output frequency range is from 10 MHz to 500 MHz.

Please see Table 13 for a full listing of input and output reference clock characteristics.

GENERAL PURPOSE I/O (GPIO) AND I2C BUS

The SV3C-DPTX provides a set of general purpose I/O (GPIO) signals that can be used for either implementing custom test vectors or for programming specialized, pre-defined functions. The pinout for the GPIO was provided in Table 4 previously. Each of the pins listed in Table 4 may be used in one of two ways:

- As configurable GPIO pins, either as inputs or outputs for "Flag" or "Trigger" functions respectively, or
- As pre-defined GPIO pins with functions including:
- "DAISY_CHAIN_TRIG_OUT" (pin 1) which can be used to synchronize the MIPI D-PHY signal outputs of two SV3C-DPTX devices, for increased lane counts
- "I2C_SCL" and "I2C_SDA" (pins 2 and 3) which implement an I2C master controller for communicating with DUT devices, and
- "Tearing Effect Input" (pin 6) for DUT testing which includes the MIPI D-PHY tearing effect.

All I/O pins are 2.5 V LVCMOS compatible, and input voltages to these pins should not exceed 2.5 V. Full specifications are given in Table 14.

Please contact Introspect for coded examples for getting started with GPIO pin functions.

Specifications

TABLE 7: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol Support			
Physical layer interface	D-PHY		
MIPI protocol	CSI, DSI		CSI-2 v1.3, CSI-2 v2.0, DSI-2 v1.1
LP/HS Handling	Automatic		Tester automatically generates LP and HS data
Ports			
Number of D-PHY Lanes	4 Lanes and CLK		
Number of Dedicated Output Reference Clocks	2		Individually synthesized frequency and output format
Number of Dedicated Input Reference Clocks	1		Used as optional external reference clock input
Number of GPIO pins	6		Via Molex connector
Number of I2C Masters	1		Via Molex connector, uses GPIO pins
Connections to PC for Introspect ESP Software Control	2		USB2 and USB3
HS Output Coupling			
Output Differential Impedance	100	Ohm	For HS operation
Differential Impedance Tolerance	+/- 10	Ohm	
Output Single-Ended Impedance	50	Ohm	For HS operation
Single-Ended Impedance Tolerance	+/- 5	Ohm	

TABLE 8: DATA RATES AND TIMING

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
HS Timing Performance			
Minimum HS Data Rate	80	Mbps	
Maximum HS Data Rate	6.5	Gbps	
Frequency Resolution of HS Data Rate	1.0	kbps	
Rise and Fall Time	< 90	ps	Typical, 20% to 80%, 1.0 Gbps, 400 mVpp differential amplitude, no preEmphasis applied, 50 ohm termination to ground
Typical Eye Opening Horizontal: Vertical:	 250 320	 ps mV	3.5 Gbps, PRBS9 pattern, 400 mVpp differential amplitude, no preEmphasis applied, 50 ohm termination to ground
Typical Eye Opening Horizontal: Vertical:	 120 200	 ps mV	6.5 Gbps, PRBS9 pattern, 400 mVpp differential amplitude, no preEmphasis applied 50 ohm termination to ground
LP Timing Performance			
Minimum LP State Period	25	ns	LP period is an integer multiple of HS period
Maximum LP State Period	240	ns	LP period is an integer multiple of HS period

TABLE 9: MIPI TRANSMITTER VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
HS Voltage Performance			
Minimum Output Voltage Swing	20	mV	Differential
Maximum Output Voltage Swing	600	mV	Differential
Voltage Swing Resolution	10	mV	Differential
Voltage Swing Accuracy	5% or 15 mV	%, mV	Larger of the percent or mV value
Minimum Common Mode Voltage	-100	mV	
Maximum Common Mode Voltage	500	mV	
Common Mode Voltage Resolution	1.0	mV	
Common Mode Voltage Accuracy	8% or 25 mV	%, mV	Larger of the percent or mV value, 0 to 500 mV programmed values
LP Voltage Controls			
Minimum Programmable LP Logic High Level	400	mV	
Maximum Programmable LP Logic High Level	1200	mV	
Minimum Programmable LP Logic Low Level	-100	mV	
Maximum Programmable LP Logic Low Level	600	mV	
Logic Level Control Resolution	1.0	mV	
Logic Level Accuracy	5% or 15 mV	%, mV	Larger of the percent or mV value

TABLE 10: MIPI TRANSMITTER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Lane Skew Performance			
Coarse Skew Range: Minimum Programmable Skew, in Integer UI	-20	UI	Lane to Lane
Coarse Skew Range: Maximum Programmable Skew, in Integer UI	+20	UI	Lane to Lane
Fine Skew Range: Minimum Programmable Skew	-500	ps	Clock to Data
Fine Skew Range: Maximum Programmable Skew	+500	ps	Clock to Data
Fine Skew Injection Resolution	1.0	ps	
Data to Clock Calibrated Offset	0.5 UI +/- 0.15 UI	UI	Default factory calibrated data to clock offset, valid across all data rates
Jitter and Noise Performance			
Maximum RJ (random Jitter) noise floor	3.5	ps RMS	Measured differentially, clock or data Data Rate from 1.0 Gbps to 6.5 Gbps
DJ (deterministic jitter) injection, minimum Frequency	0.1	kHz	Sinusoidal jitter
DJ injection, maximum frequency	50	MHz	Sinusoidal jitter
DJ injection, frequency resolution	0.1	kHz	
DJ injection, maximum magnitude	2	UI pp	1 MHz frequency jitter Tested to a maximum of 1000 ps
DJ injection, magnitude resolution	500	fs	
DJ injection, accuracy	10% or 10 ps	%, ps	Larger of the percent or ps value

TABLE 11: PATTERN MEMORY AND SEQUENCING

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
User-Programmable Pattern Memory			
Minimum Pattern Segment Size	8	Bits	
Maximum Pattern Segment Size	4	GBytes	For additional memory, contact Introspect
Total Memory Space for Transmitters	4	GBytes	For additional memory, contact Introspect
Pattern Sequencer			
Sequence Control	Yes		Loop infinite Loop-on-count (see count below) Play to end
Number of Sequencer Slots per Pattern Generator	16		Each pattern generator can string up to 16 different segments together, each with its own repeat count
Number of Entry Slots	1		Separate from above 16 segments
Number of Exit Slots	1		Separate from above 16 segments
Maximum Repeat Count Per Slot	65536		
Maximum Repeat Count for Outer Loop	65536		Outer loop can encompass any number of slots
Additional Pattern Characteristics			
Escape Mode Command Entry	Yes		Per lane
Pattern Switching	Yes		Wait to end of segment, or immediate

TABLE 12: DATA FORMATS AND MIPI PROTOCOL FEATURES

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Supported Pixel Formats			
Supported Pixel Formats (CSI)	RAW, RGB, YUV		RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, RGB444, RGB555, RGB565, RGB666, RGB888, YUV420, YUV422
Supported Pixel Formats (DSI)	RGB YCbCr		RGB101010, RGB121212, RGB332, RGB565, RGB666, RGB888, YCbCr420_12bit, YCbCr422_16bit, YCbCr422_20bit, YCbCr422_24bit
Supported Features			
ALP support (CSI)	Yes		
EDP support (CSI)	Yes		
Display Command Set (DSI)	Yes		
Data Compression (DSI)	Yes		DSC, V-DCM
Data Scrambling (DSI)	Yes		Data payload and footer
Tearing Effect (DSI)	Yes		
Bus-Turn Around	Yes		CSI and DSI
Virtual Channel Support	Yes		CSI and DSI
Packet Error Insertion	Yes		CSI and DSI

TABLE 13: REFERENCE CLOCK CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Reference Clocks			
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Frequency Resolution of Programmed Data Rate	1	kHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	500	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Output Clock I/O Standards			LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 14: GPIO AND I2C BUS VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	2.5	V	All GPIOs operate at 2.5 V LVCMOS
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.7	V	
V_{IH} minimum	1.7	V	
V_{IH} maximum	2.5	V	
V_{OL} maximum	0.4	V	
V_{OH} minimum	2.0	V	

TABLE 15: PHYSICAL CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Dimensions			
Length	9.5, 242	in, mm	
Width	4.25, 108	in, mm	
Height	1.3, 34	in, mm	
Weight	2	lbs	
Physical Connections			
Lane 1 to Lane 4, Clock	MXP		Huber & Suhner, 16 pin
GPIO			Available through 12 pin header Molex 15-91-2125
Ref Clock In	SMP		SMP Differential Pair
Ref Clock Out	SMP		SMP Differential Pair
PC connection	USB2 USB3		USB2.0 mini B USB3.0 micro B
Power Switch / Connector			AC adapter provided 110/220 V, 50/60 Hz
Power Consumption			
DC Input Voltage	12	Volt	
Current Draw	4.2	Amp	6.5 Gbps / 4 Lane, HS-only pattern
Current Draw	3.6	Amp	3.5 Gbps / 4 Lane, HS-only pattern

REVISION NUMBER	HISTORY	DATE
1.0	Document creation	July 26, 2014
1.1	Updated document template	June 4, 2015
1.2	Updated voltage specifications	January 29, 2016
1.3	Updated data rate specifications, adding ordering information	April 20, 2018
1.4	Updated Figure 5 and Table 3; added Table 6	June 20, 2018
1.5	Updated document template, updated voltage and timing specifications, general feature description updates.	June 7, 2021
1.6	Updated document template, updated voltage and timing specifications.	July 5, 2021

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