

SV4E-DPRXCPRX MIPI Receive Device Emulator

PRODUCT BRIEF

System-Level Tester for Validating MIPI Transmitters



Figure 1. Introspect's SV4E-DPRXCPRX system-level tester (140 mm x 89 mm)

The SV4E is a highly-integrated system-level tester that facilitates the rapid screening, calibration, and optimization of MIPI® Alliance enabled devices. Such devices include high-resolution image sensors, camera modules, and advanced image signal processors used in mobile or IoT applications. The SV4E-DPRXCPRX features a unique dual-mode D-PHYSM/C-PHYSM analog front-end. It also integrates reconfigurable protocol stacks for the CSI-2SM standards. These features make it incredibly easy to create a realistic test setup for tuning and calibrating system parameters such as camera colour settings or noise performance.

FEATURES

- Integrated PHY: truly compact design that can act as a D-PHY or a C-PHY receiver
- **High bandwidth:** up to 2.5 Gbps D-PHY signaling and 2.5 Gsps C-PHY signaling per lane; up to 4 lanes per port
- Native protocol implementation: true CSI-2 controller instantiation with support for version 2.1 specifications
- **Easy to use:** Introspect ESP Software enables interactive operation or full automation

BENEFITS

- Future proof: protect your investment by adopting a high-performance tool for multiple product applications and across a large span of data rates
- Self-contained: an all-in-one system enables true protocol capture and helps create a system-oriented testing methodology
- Automated: scripting capability is ideal for debug tasks and full-fledged production screening of devices and system modules

Typical Application: Image Sensor Testing at 2.5 Gbps



Figure 2. SV4E-DPRXCPRX testing a C-PHY camera module



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Protocol and Signal Parameters

Feature	Description	Benefit
Application / Protocol Support	D-PHY version 1.1, 1.2, 2.0 (including BTA) C-PHY version 1.0, 1.1 (including BTA) CSI-2 version 1.3, 2.0, 2.1	Able to capture device transmissions from varied application contexts including ADAS sensors and bridge devices.
Receive Payload Support	PRBS packet loop patterns HS-only and LP-only patterns Arbitrary video patterns at any frame rate	Detects a wide spectrum of data conditions for the purposes of debug or colour calibration during production

Key Performance Parameters

Parameter	Value	Description
Lane Count	4 lanes of D-PHY; 3 lanes of C-PHY	Allows for deployment into multiple generations of products or multiple product families
Data Rates	80 Mbps to 2.5 Gbps in D-PHY mode; 80 Msps to 2.5 Gsps in C-PHY mode	Allows for supporting high- performance applications
GPIO	DUT reset control pin 15 user programmable IO pins	Provides full control over devices under test
Auxiliary Power	Up to 6 DC outputs with CMU capability	Enables complete module test and DC measurement capability

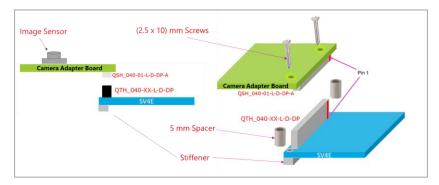


Figure 3. Mechanical connection to camera adapter board



Figure 4. Software interface for confirming received image frames