PCIE GEN5 U.3 TO U.2 ADAPTER

FORM FACTOR

Have an adapter board which goes between an U.2 Drive and U.3 enclosure, the adapter board will take the pinout from U.2 changing it to the pin out of U.3 which will allow the U.2 drive to function in the U.3 enclosure. Both adapters QTL3064 and QTL3065 with Flex Cable will follow similar Quarch products formfactor (Dimensions of the board can be found in appendix C.). The QTL3065 version of the board will also be able to tap into the SMBDAT and SMBCLK signals coming off the adapter board by a flexible cable.

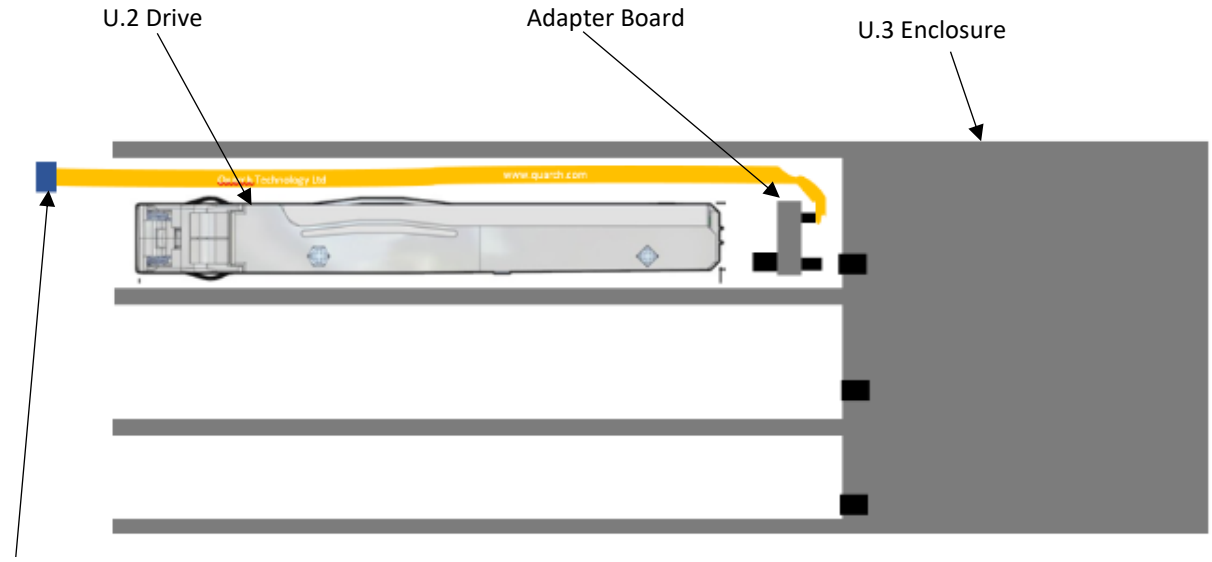


Figure 1 - Operation

PIN ALLOCATION

The QTL3065 adapter board will have jumpers on the SMBDAT and SMBCLK signals which will pass straight through the adapter board when the jumpers are connected, with the ability to monitor the bus using the flexible cable. When the jumpers are removed from J6 and J7, these signals are broken between the host and device leaving the flexible cable connect to the device side only allowing signals to be sent down into the device. To allow a connection to the SMBUS on the end of the flexible cable there is a Clincher Receptacle (65801-008) on the end of the flexible cable, shown in figure 1. The socket on this receptacle has a 0.81mm opening and can fit 0.025-inch square pins in.

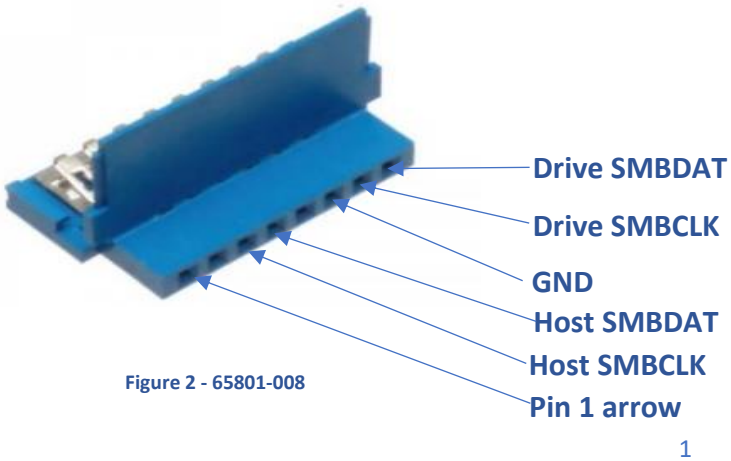


Figure 2 - 65801-008

Both U.2 and U.3 use PCIe protocol, the main difference between them is the pin out on the connectors even although both use the same physical connector. The adapter board takes the pin out from the U.2 device and re-routes these through the adapter board into the pin out for the U.3 enclosure (Appendix A).

U.2 only has one Ifdet# pin whereas U.3 has 2, these pins are used so the host knows what type of device is inserted. To allow the U.2 drive to work in the U.3 enclose the IfDet# pin is connected to both IfDet# and IfDet2# on the U.3 enclose as this will cause the enclose to think it has a SSF-TA-1001 drive inserted, and with the re-routed pin out the U.2 will work as desired, table showing the combinations of these pins can be found in Appendix B.

U.3 has two Host Port Type (HPT) pins which the device can use so it knows what sort of enclose it is on. However, U.2 does not make use of these pins and since these pins come for the host to the drive, we can leave these disconnected and the U.2 drive will still work as desired.

ADAPTER BOARD VARIANTS

QTL3064 – GEN5 PCIE U.3 TO U.2 ADAPTER - NO CABLE

This board functions as a standard adapter. This version of the board does not include the flex cable. The R1 and R2 resistors ensure continuity for the SMBCLK and SMBDAT lines, respectively. Different sideband signals can be tapped at the J4 connector pads. Refer to the table in Appendix D.

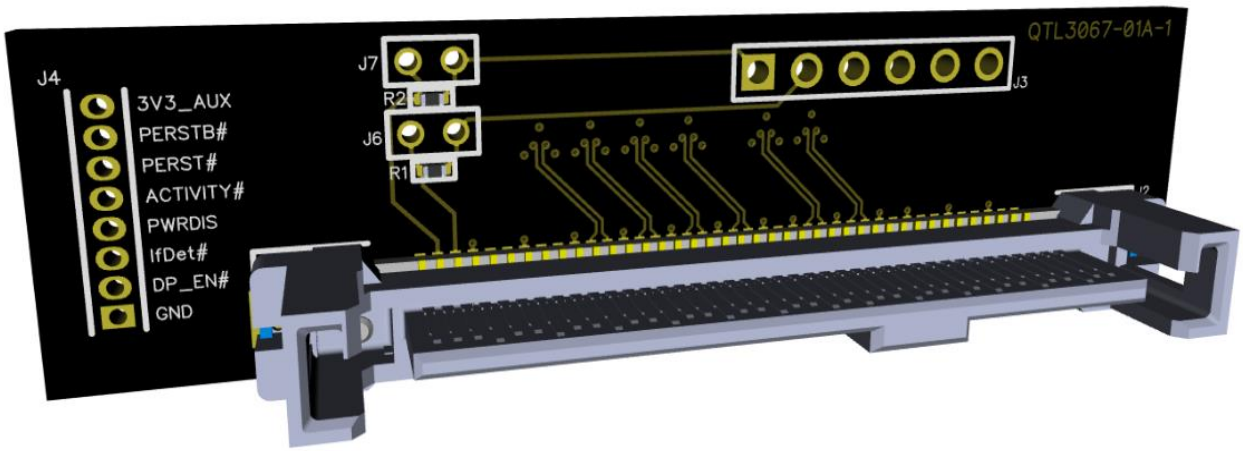


Figure 3 - QTL3064

GEN5 PCIE U.3 TO U.2 ADAPTER + FLEX CABLE

This is the same as the standard adapter board shown in Figure 3, but with two additional components attached, allowing the SMBCLK and SMBDAT signals to be monitored, as explained in the PIN allocation section. Jumpers on J6 and J7 headers ensure continuity for the SMBCLK and SMBDAT lines, respectively.

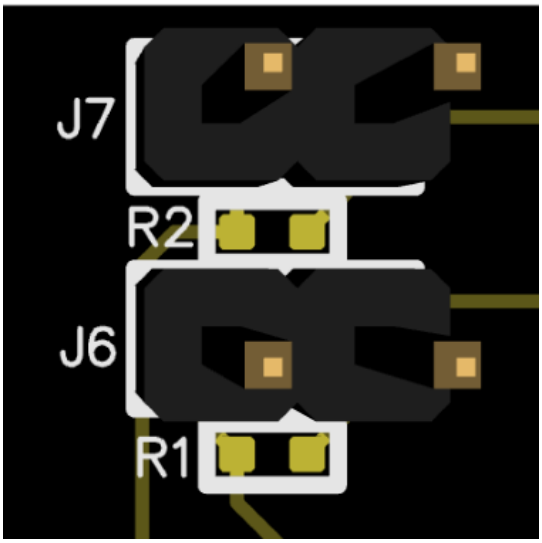


Figure 4 - J6 and J7 headers

APPENDIX A

U.2 Receptacle pin out to U.3 Plug pin out		
U.2 Pin	**Signal**	**U.3 Pin**
P1	WAKE#	P1
P2	-	NC
P3	PWRDIS	P3
P4	IfDet#	P4, E6
P5	GND	P5
P6	GND	P6
P7	5V Charge	NC
P8	5V	NC
P9	5V	NC
P10	PRSNT#	P10
P11	ACTIVITY#	P11
P12	GND	P12
P13	12V Charge	P13
P14	12V	P14
P15	12V	P15
S1	GND	S1
S2	-	NC
S3	-	NC
S4	GND	S4
S5	-	NC
S6	-	NC
S7	GND	S7
S8	GND	S8
S9	-	NC
S10	-	NC
S11	GND	S11
S12	-	NC
S13	-	NC
S14	GND	S14
S15	Reserved	NC
S16	GND	S16
S17	PETp1	S9
S18	PETn1	S10
S19	GND	S19
S20	PERn1	S12
S21	PERp1	S13
S22	GND	S22
S23	PETp2	S17
S24	PETn2	S18
S25	GND	S25
S26	PERn2	S20
S27	PERp2	S21
S28	GND	S28

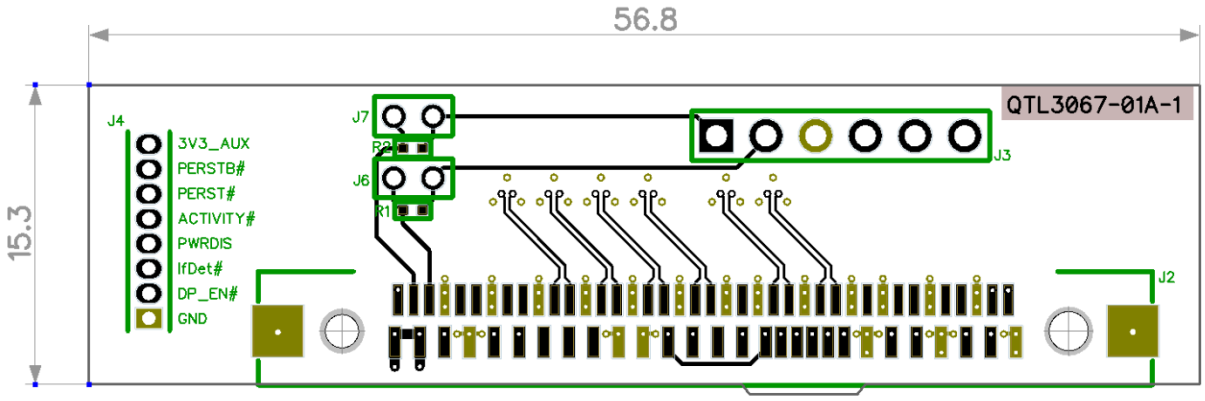
E1	REFCLKB+	E1
E2	REFCLKB-	E2
E3	3V3 AUX	E3
E4	CLKREQ#/PERSTB#	E4
E5	PERST#	E5
E6	Reserved	NC
E7	REFCLK+	E7
E8	REFCLK-	E8
E9	GND	E9
E10	PETp0	S2
E11	PETn0	S3
E12	GND	E12
E13	PERn0	S5
E14	PERp0	S6
E15	GND	E15
E16	Reserved	NC
E17	PETp3	S23
E18	PERn3	S24
E19	GND	E19
E20	PERn3	S26
E21	PERp3	S27
E22	GND	E22
E23	SMBCLK	E23
E24	SMBDAT	E24
E25	DuelPortEn#	E25

APPENDIX B

U.3			
PRSNT#	IfDet#	IfDet2#	
P10	P4	E6	
GND	GND	OPEN	SAS/ SATA
GND	OPEN	OPEN	Undefined
OPEN	GND	OPEN	Quad PCIe
OPEN	OPEN	OPEN	Bay Empty
GND	GND	GND	Undefined
GND	OPEN	GND	Undefined
OPEN	GND	GND	SFF-TA-1001 PCIe
OPEN	OPEN	GND	Gen-Z

U.2			
PRSNT#	IfDet#	NC	
P10	P4	E6	
de-asserted	Active Low		SFF-8639
All other combinations			Out of Spec

APPENDIX C



*All sizes in mm.

**Board thickness is 1.6mm.

APPENDIX D

J.4 Pads	
3V3_AUX	Provides a 3.3V auxiliary power supply to the device.
PERSTB#	Resets the secondary PCIe interface (active low).
PERST#	Resets the primary PCIe interface (active low).
ACTIVITY#	Indicates device activity (active low).
PWRDIS	Disables power to the device when asserted.
IfDet#	Interface detection signal (active low).
DP_EN#	Enables Dual Port functionality (active low).
GND	Ground connection.